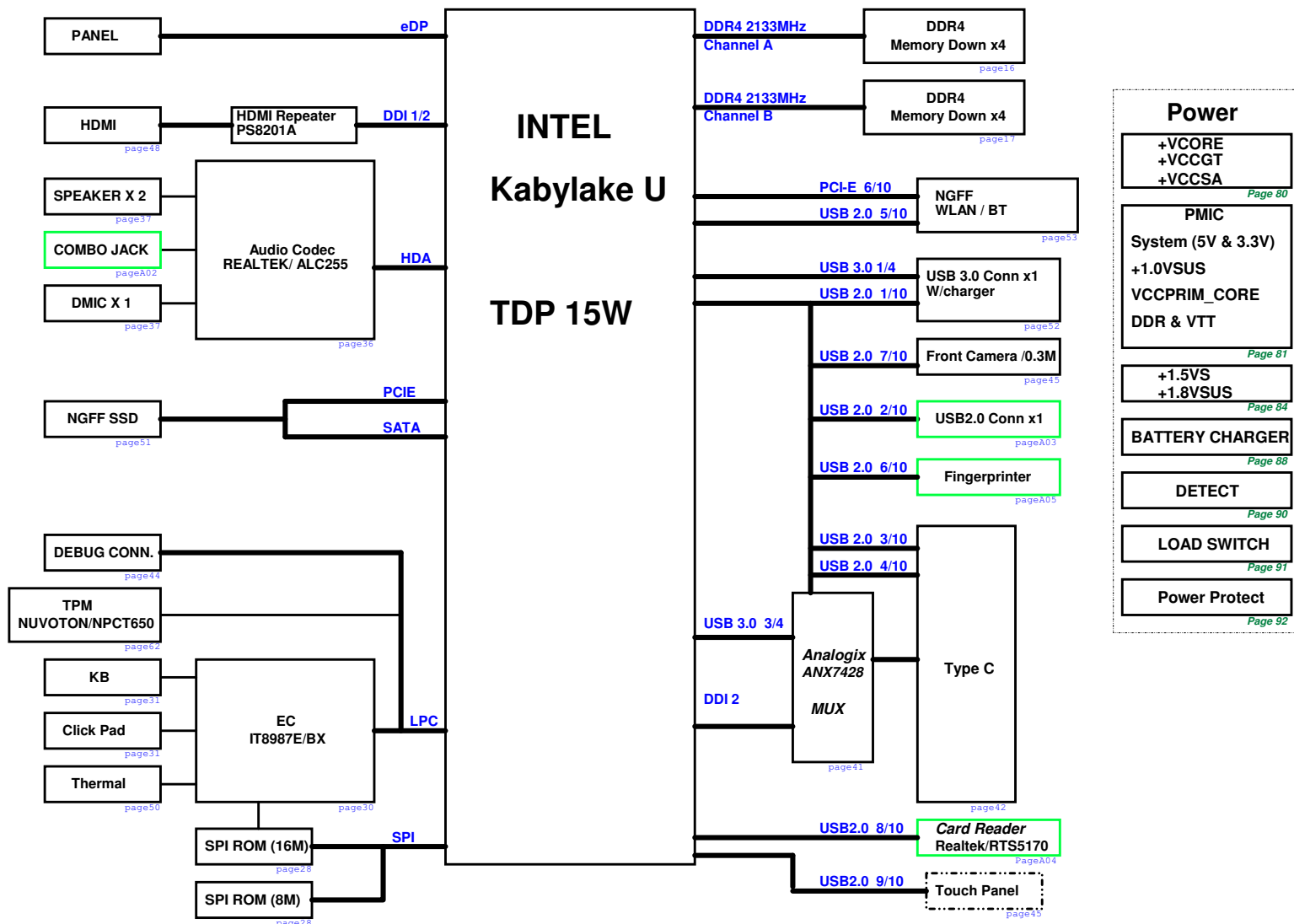


01. Block Diagram  
02. GPIO Setting  
03. CPU(1)\_DDI/eDP  
04. CPU(2)\_DDR4  
05. CPU(3)\_+VCCCORE  
06. CPU(4)\_+VCCGT  
07. CPU(5)\_+VDDQ/IO/SA  
08. CPU(6)\_CPU GND  
09. CPU(7)\_CFG/RSVD  
15. DDR4(0)\_Termination  
16. DDR4(1)\_CH0  
17. DDR4(2)\_CH1  
19. DDR4(4)\_CA/DQ Voltage  
20. PCH(1)\_SPI/LPC  
21. PCH(2)\_ISH  
22. PCH(3)\_HDA/SDIO  
23. PCH(4)\_USB/PCIE/SATA  
24. PCH(5)\_CLK/RTC  
25. PCH(6)\_POWER MANAGEMENT  
26. PCH(7)\_POWER  
28. PCH(9)\_SPI/SMB  
30. EC\_IT8587/FX  
31. EC\_IT8587/FX\_KB/TP/KBBL  
32. RST\_Reset Circuit  
36. AUD\_ALC255  
37. AUD(2)\_SPK/DMIC  
41. USB\_Type-C ANX7428  
42. USB Type-C Receptacle  
43. USB Type-C Dead Battery  
44. Debug CONN  
45. CRT(1)\_eDP,CAMERA,TSN  
47. HDMI Repeater PS8201A  
48. HDMI OUT  
50. THERMAL / FAN  
51. NGFF PCIE\*4/SATA SSD  
52. USB 3.0/Sleep Charge IC  
53. NGFF PCIE WLAN/BT  
56. LED  
57. Discharge  
60. DC\_DC/BAT CONN  
62. TPM NPCT650  
64. IO Board  
65. ME\_CONN / Skew Hole  
68. BYPASS EC SEQUENCE  
80. POWER\_VCORE for U22  
81. POWER\_SYSTEM  
82. POWER\_+1.0VSUS  
83. POWER\_DDR & VTT\_UMA  
84. POWER\_1.8VSUS  
85. POWER\_1.5VS  
86. POWER\_XXX  
87. POWER\_XXX  
88. POWER\_CHARGER  
89. POWER\_AC\_PD\_WC Input  
90. POWER\_DETECT  
91. POWER\_LOAD SWITCH  
92. POWER\_PROTECT  
93. POWER\_SIGNAL  
94. POWER\_FLOWCHART  
A02. AUD(2)\_JACK  
A03. USB20  
A04. CB\_RTSS170\_GR

# 14" CARDB(X3) & M3RDA(M3) for Kabylake U Platform Block Diagram



Discharge Circuit

Page 57

DC &amp; BATT. Conn.

Page 60

Reset Circuit

Page 32

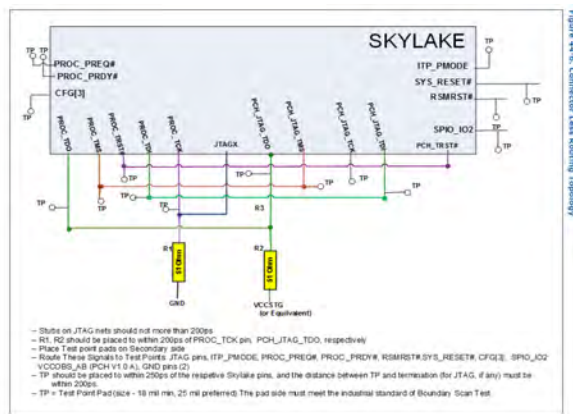
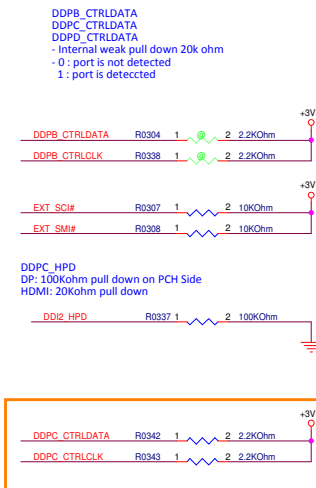
Skew Holes

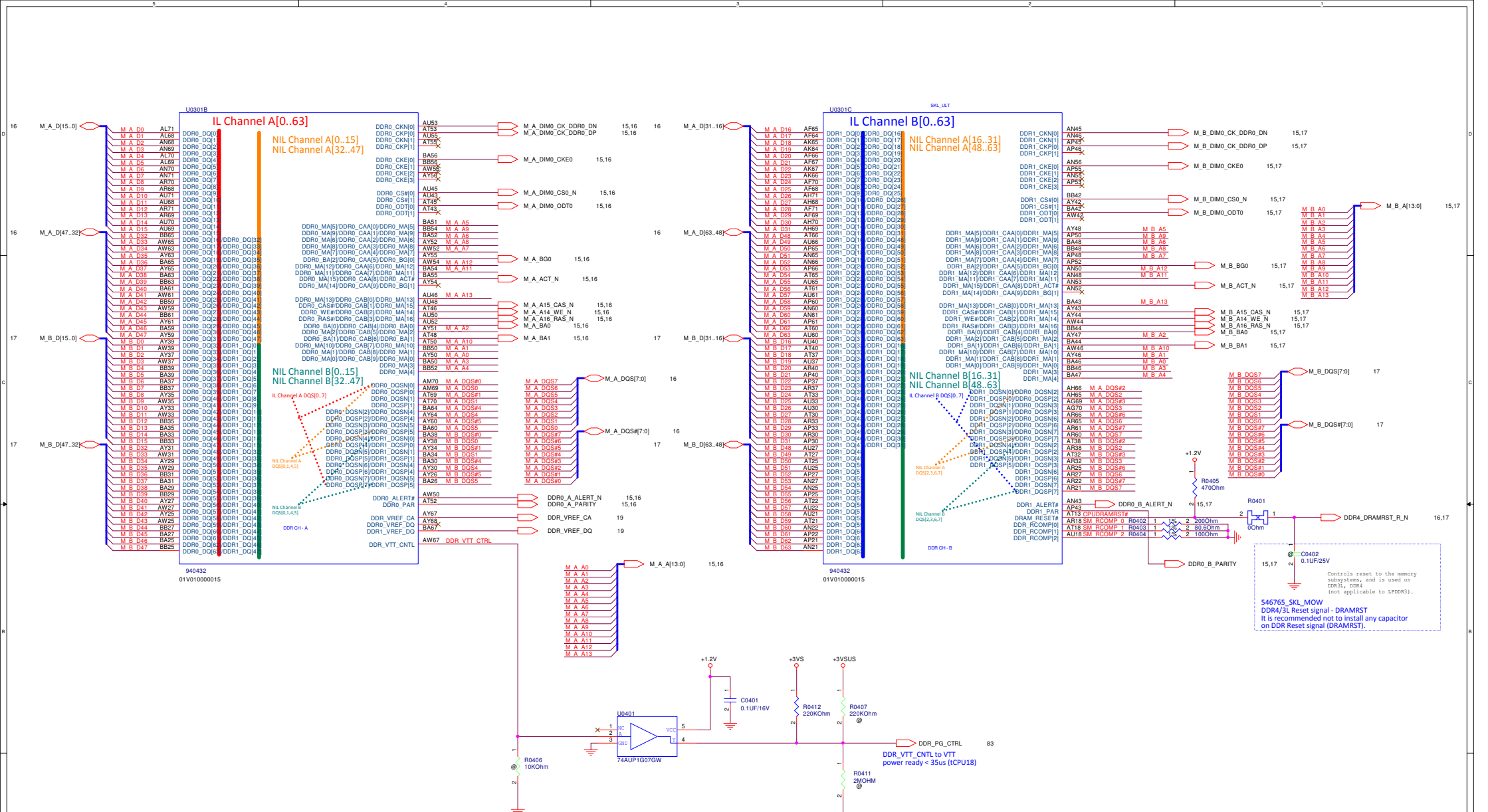
Page 65

&lt;Variant Name&gt;

<b>PEGATRON</b>		Title : <b>Block Diagram</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG14HW3</b>		Engineer: <b>Andy Kao</b>	
Size	Project Name	Rev	
Custom	<b>X3</b>	1.0	
Date: <b>Friday, October 21, 2016</b>		Sheet	1 of 97

5	4	3	2	1				
EC GPIO	Use As	Signal Name	EC GPIO	Use As	Signal Name	EC GPIO	Use As	Signal Name





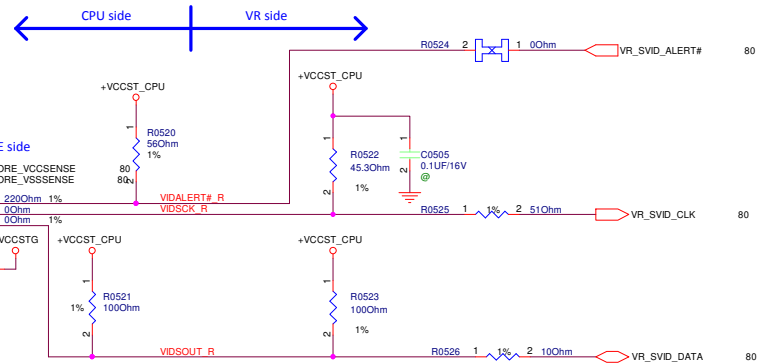
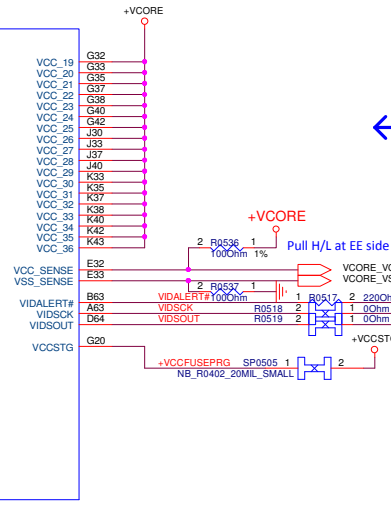
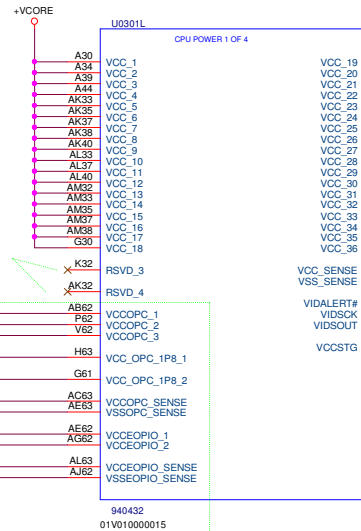
Symbol U0301 B		Symbol U0301 C	
interleaved(Symbol default)	Non-interleaved	interleaved(Symbol default)	Non-interleaved
BYTE 0	ChannelA DQ[0..63] DQS/DQS#[0..7]	BYTE 0	ChannelA DQ[16..31] DQS/DQS#[2,3]
BYTE 1		BYTE 1	ChannelADQ[48..63] DQS/DQS#[6,7]
BYTE 2		BYTE 2	ChannelB DQ[0..63] DQS/DQS#[0..7]
BYTE 3		BYTE 3	ChannelB DQ[16..31] DQS/DQS#[2,3]
BYTE 4		BYTE 4	ChannelB DQ[48..63] DQS/DQS#[6,7]
BYTE 5	ChannelB DQ[0..15] DQS/DQS#[0,1]	BYTE 5	
BYTE 6		BYTE 6	
BYTE 7		BYTE 7	

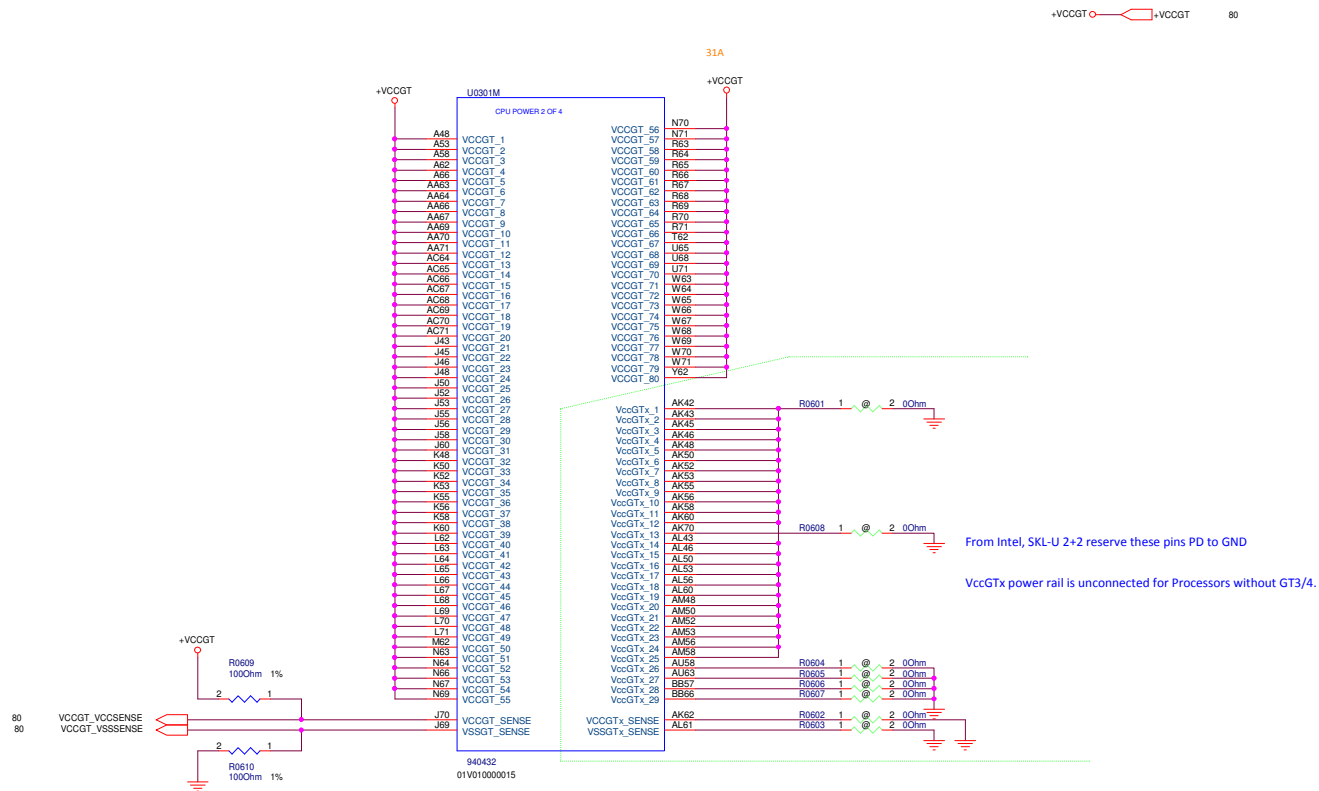
SKL 2+2, +V1.8VS\_EDRAM / +V\_EDRAM\_VR / +V\_EOPIO\_VR  
From Intel, SKL-U 2+2 reserve these pins PD to GND

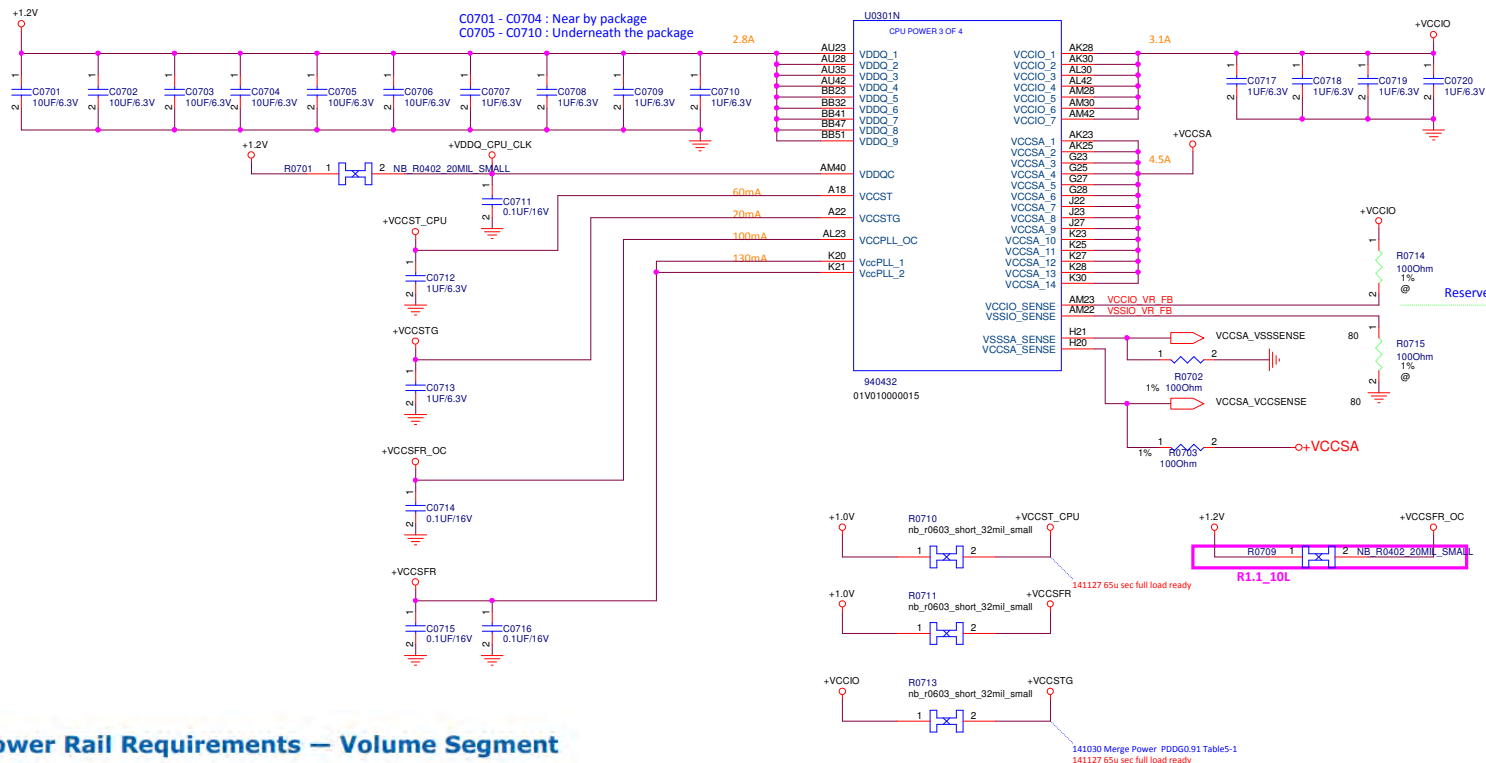
RSVD NC

+V CORE 80  
+VCCSTG 3,7  
+VCCST\_CPU 3,7,9,25,32

29A



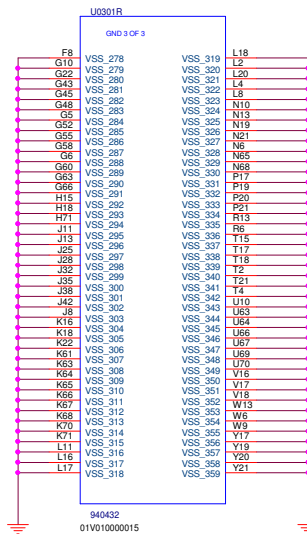
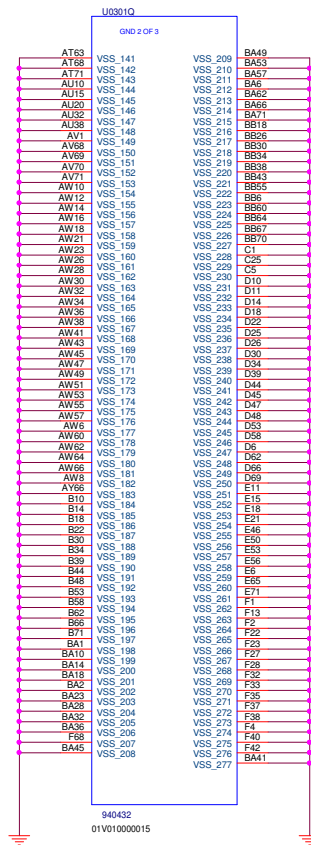
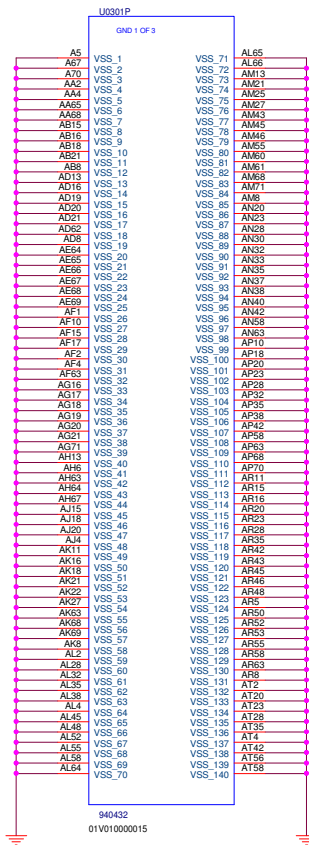




**Table 5-1. Power Rail Requirements — Volume Segment — U-Line**

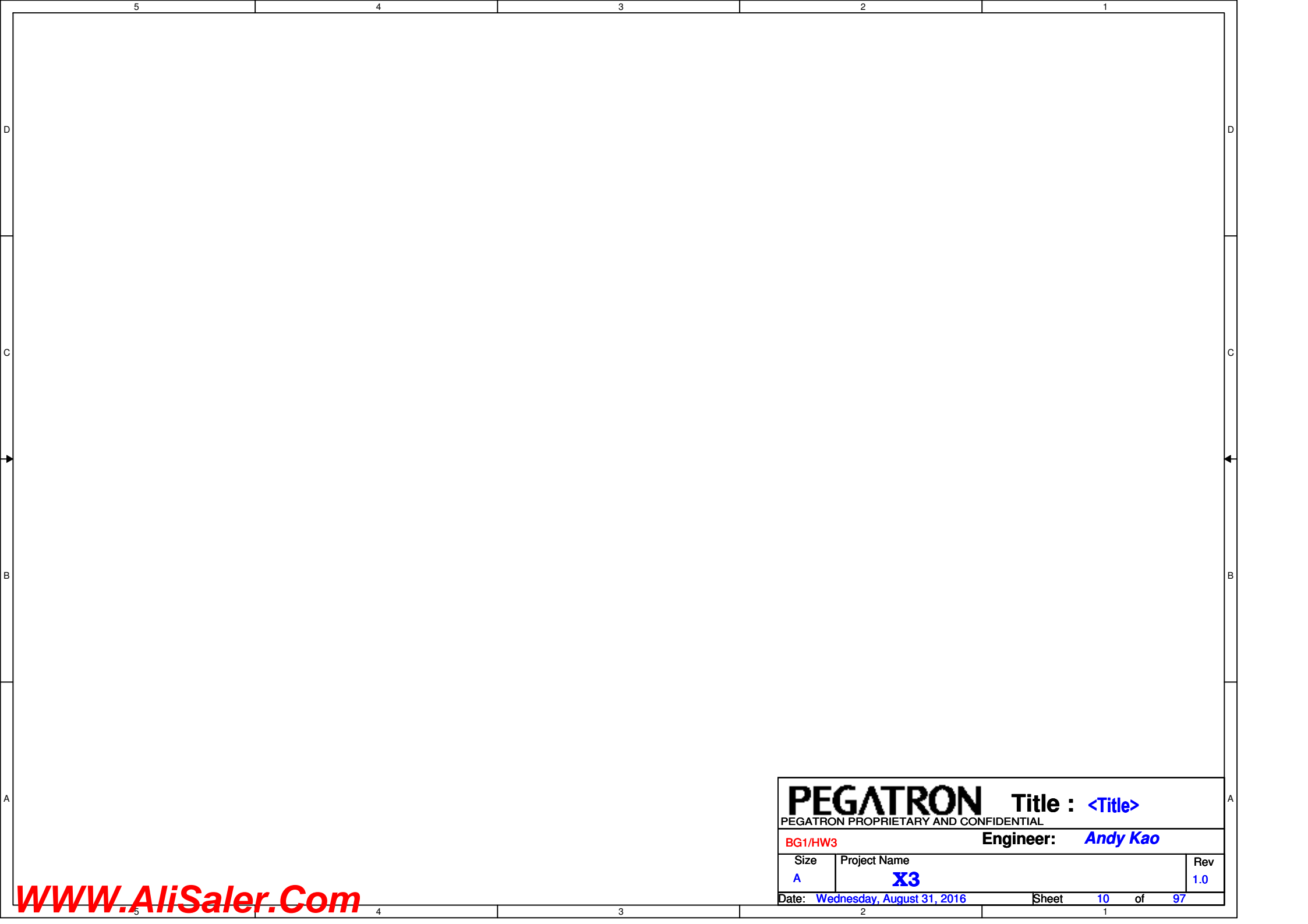
Load switch (LS)	LS ENABLE	Load/Rail name	I <sub>max</sub> (A)
<= 65usec full load ready (Note 16)	SLP_S4#	VCC <sub>ST</sub>	0.04
		VCC <sub>PLL</sub> (VCC <sub>SFR</sub> )	0.12
<= 65usec full load ready	SLP_S3# AND SLP_S0#	VCC <sub>IO</sub>	3.0
		VCC <sub>STG</sub>	0.04

16. VCCST ramp time can potentially be slowed than listed, depending on platform design. However, all timings documented in the PSS chapter must be met, specifically T<sub>cpu\_04</sub>









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<b>PEGATRON</b> <b>Title :</b> <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>
Size <i>A</i>	Project Name <b>X3</b>	Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>10</i> of <i>97</i>

**PEGATRON** Title : <Title>

**BG1/HW3**      **Engineer:** *Andy Kao*

Size <b>A</b>	Project Name <b>X3</b>	Rev <b>1.0</b>
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Date: Wednesday, August 31, 2016	Sheet 11 of 97
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D

C

B

A

**PEGATRON** Title : <Title>

**PEGATRON PROPRIETARY AND CONFIDENTIAL**

BG1/HW3

**Engineer:** *Andy Kao*

Size

A

Project Name
--------------

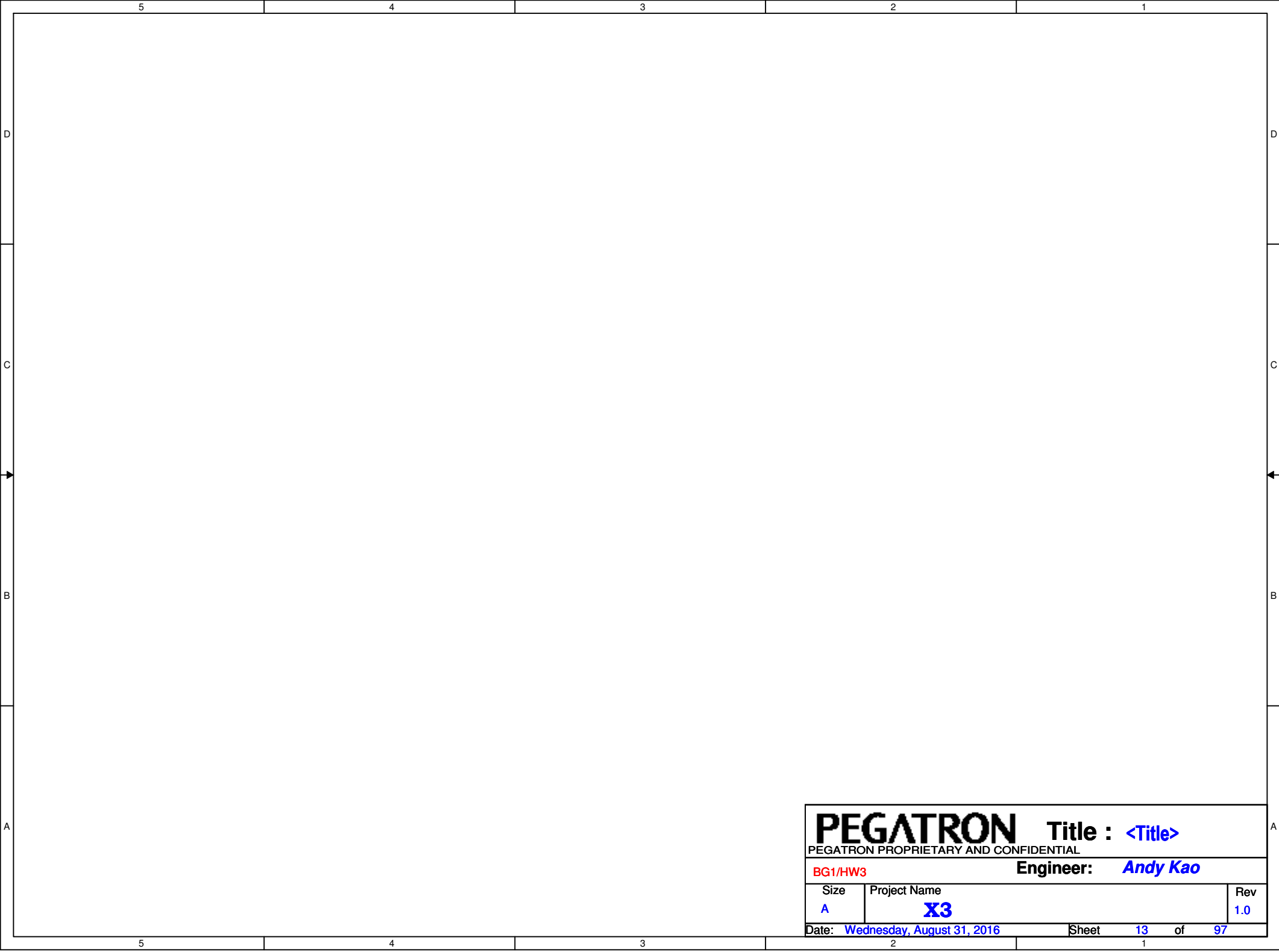
### X3

Rev

1.0

Date: Wednesday, August 31, 2016

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<b>PEGATRON</b>		<b>Title :</b> <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>	
Size	Project Name		Rev
<i>A</i>	<i>X3</i>		<i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>13</i> of <i>97</i>	

D

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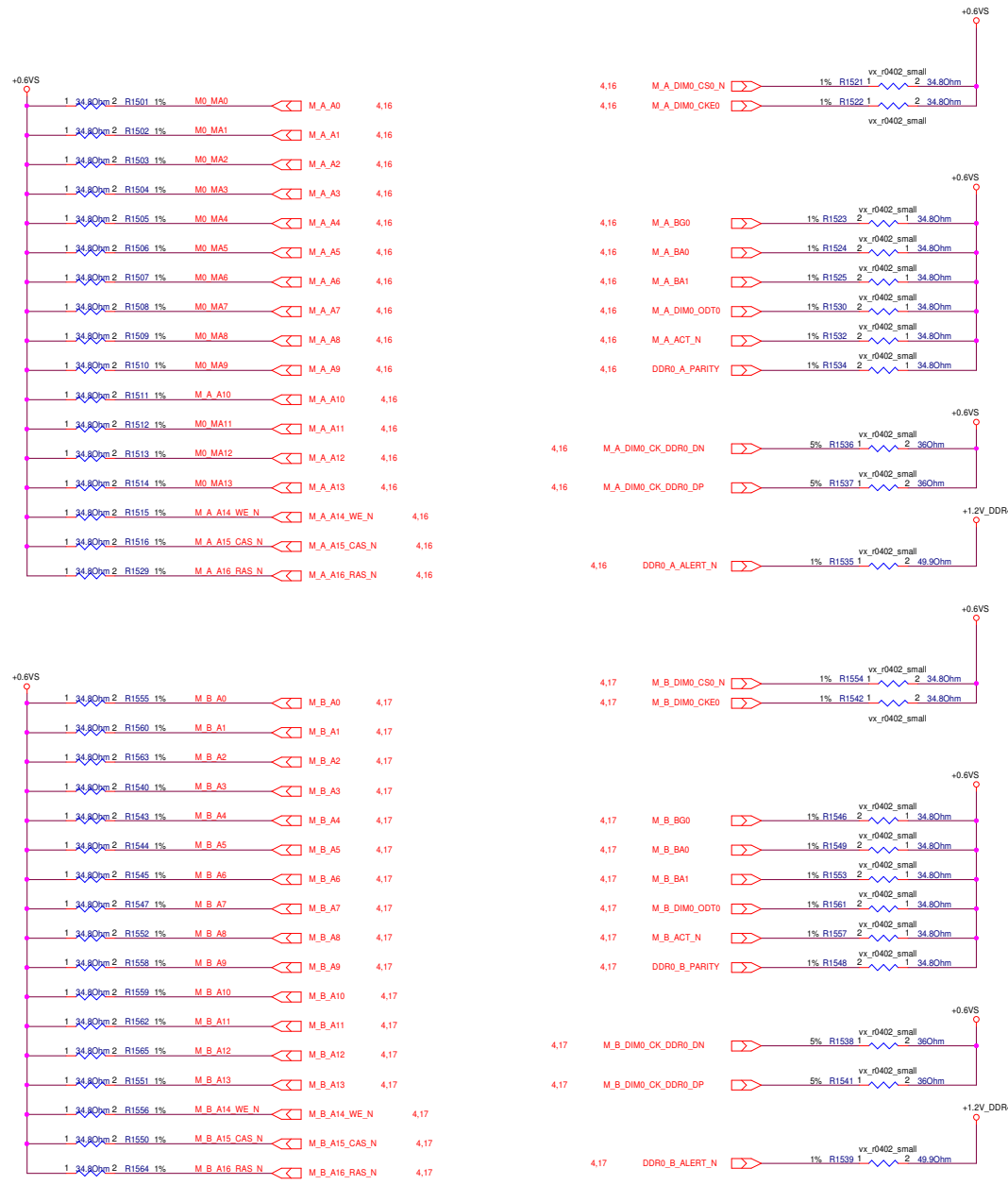
BG1/HW3 Engineer: *Andy Kao*

Size	Project Name	Rev
A	X3	1.0

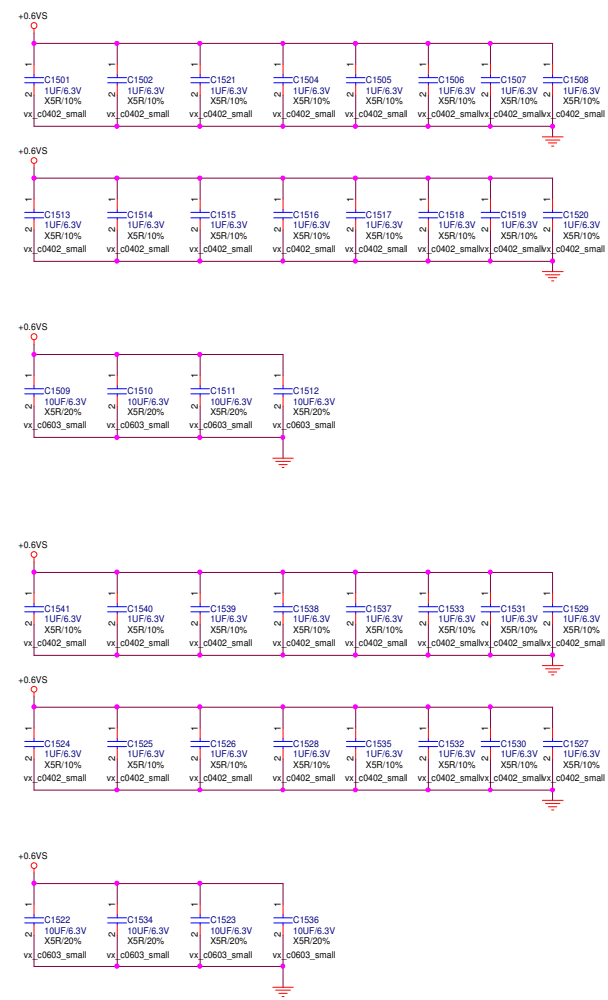
Date: Wednesday, August 31, 2016 Sheet 14 of 97

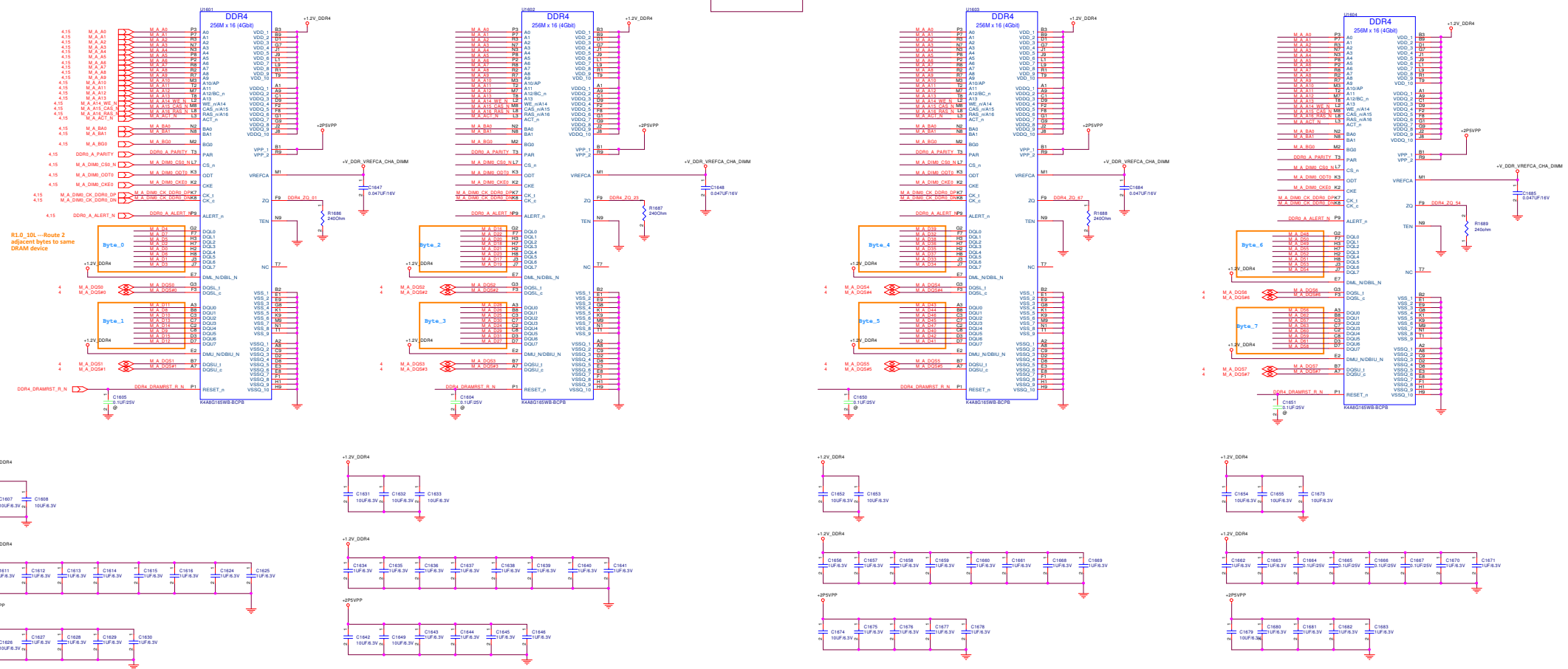
# DDR4(0)\_Termination

+0.6VS  +0.6VS 57,83  
+1.2V\_DDR4  +1.2V\_DDR4 4,7,16,17,19,57,83



Average placed close to +VDDQ\_VTT power plane









D

C

B

A

D

C

B

A

**PEGATRON**      Title : **<Title>**

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

**Engineer:** *Andy Kao*

Size

**A**

Project Name	
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### X3

Rev
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1.0

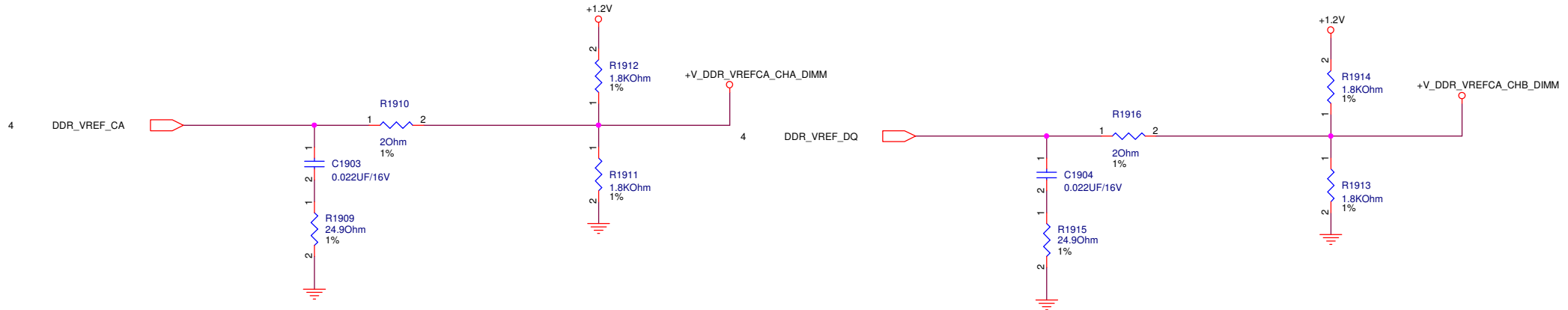
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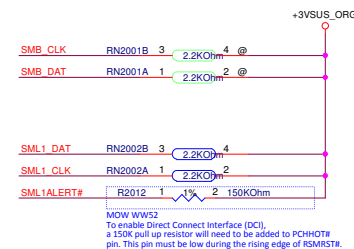
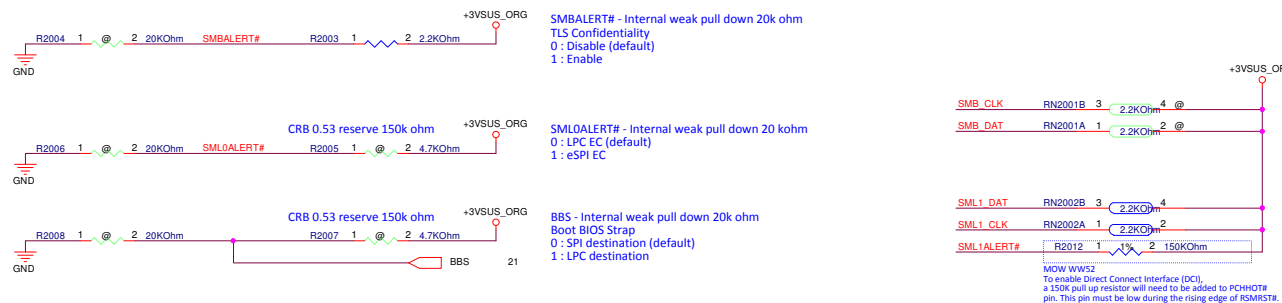
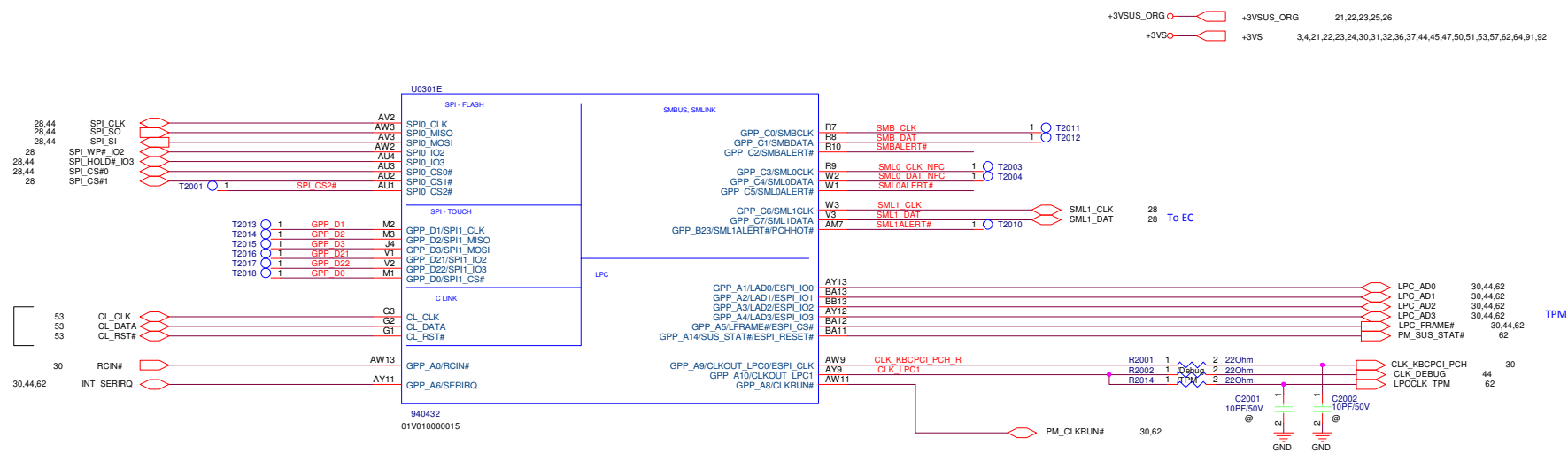
# DDR4(3)\_CA/DQ Voltage

+1.2V		+1.2V	4,7,15,16,17,57,83
+V_DDR_VREFCA_CHB_DIMM		+V_DDR_VREFCA_CHB_DIMM	17
+V_DDR_VREFCA_CHA_DIMM		+V_DDR_VREFCA_CHA_DIMM	16

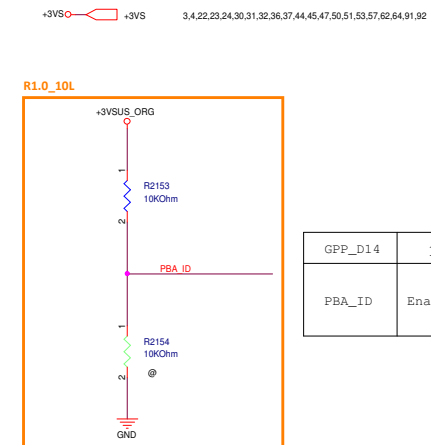
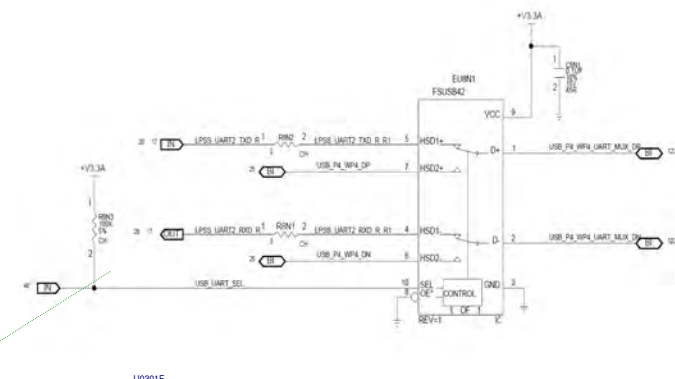
## DDR4 Vref (Intel Schematic Review)



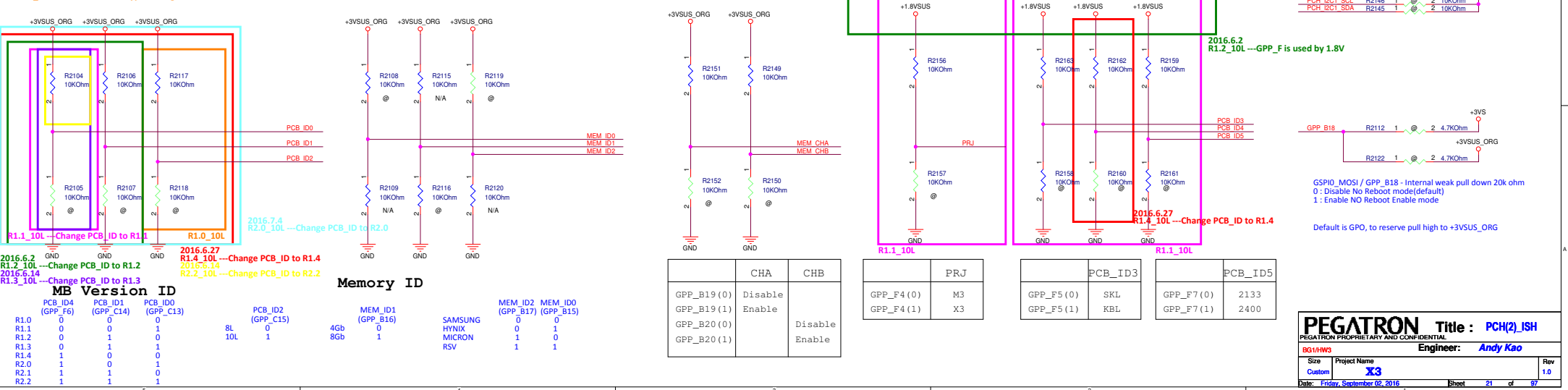
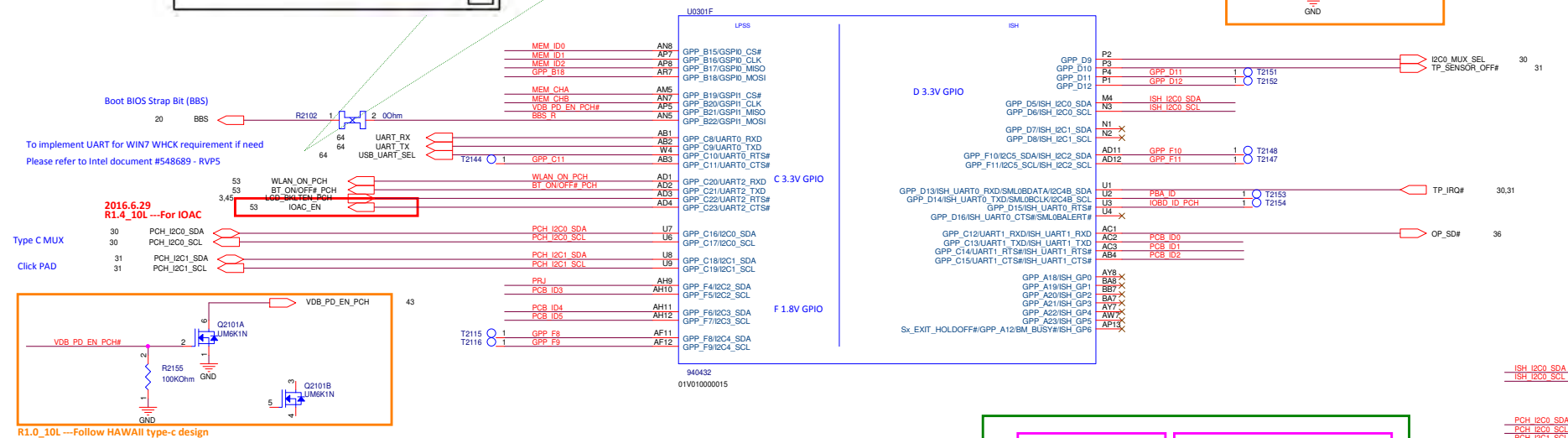
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<b>PEGATRON</b> Title : <b>DDR3(3)_CA/DQ Voltage</b>		
BG1/HW3 Engineer: <b>Andy Kao</b>		
Size B	Project Name <b>X3</b>	Rev 1.0
Date: <b>Wednesday, August 31, 2016</b> Sheet <b>19</b> of <b>97</b>		



With skylake EHCI Removal, Potential Gap with Windows\* 7 Kernel Debug and OS Installation – Mitigation Required



GPP_D14	1	0
PBA_ID	Enable	Disabl



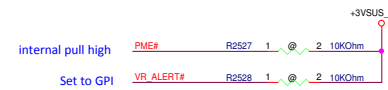
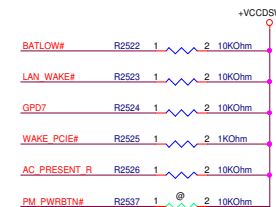
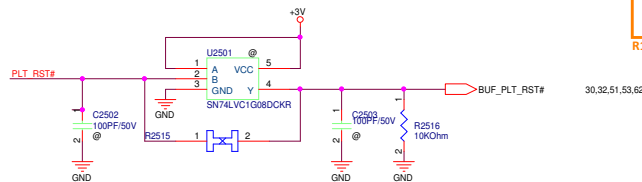
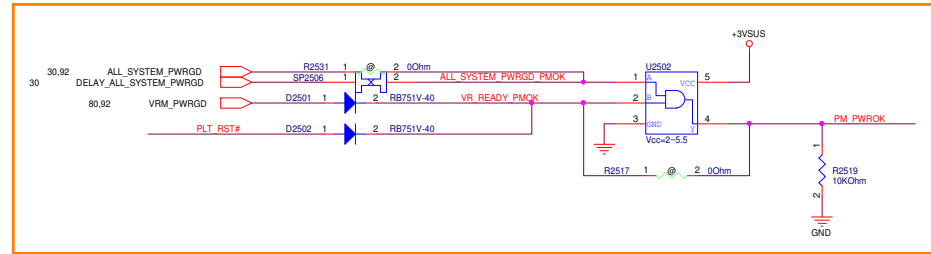
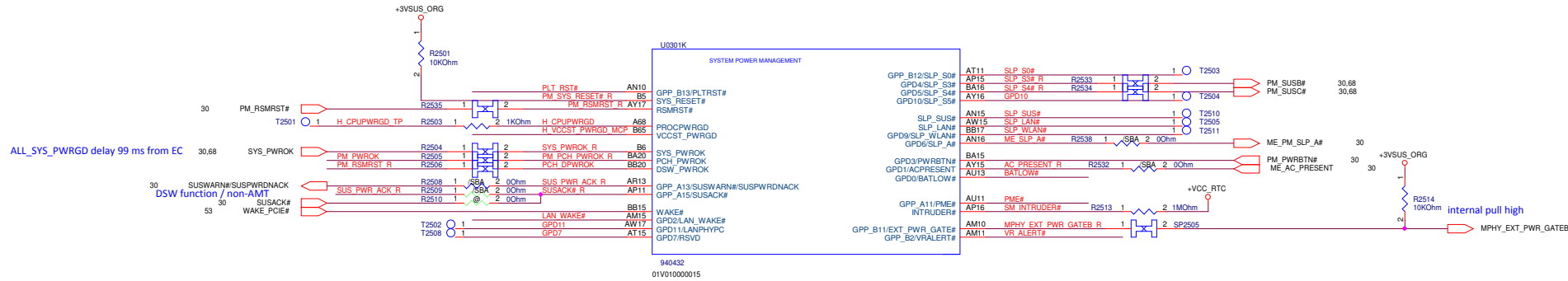




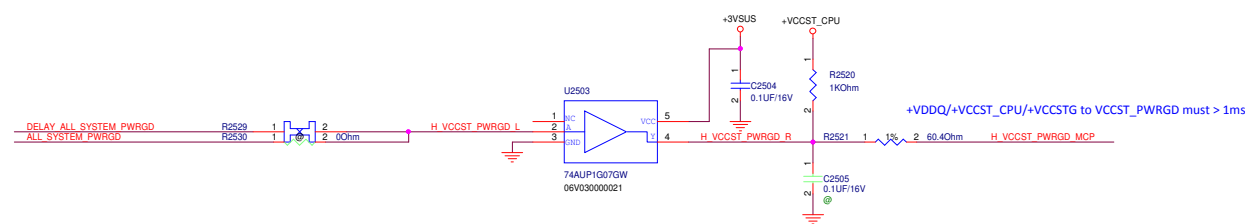




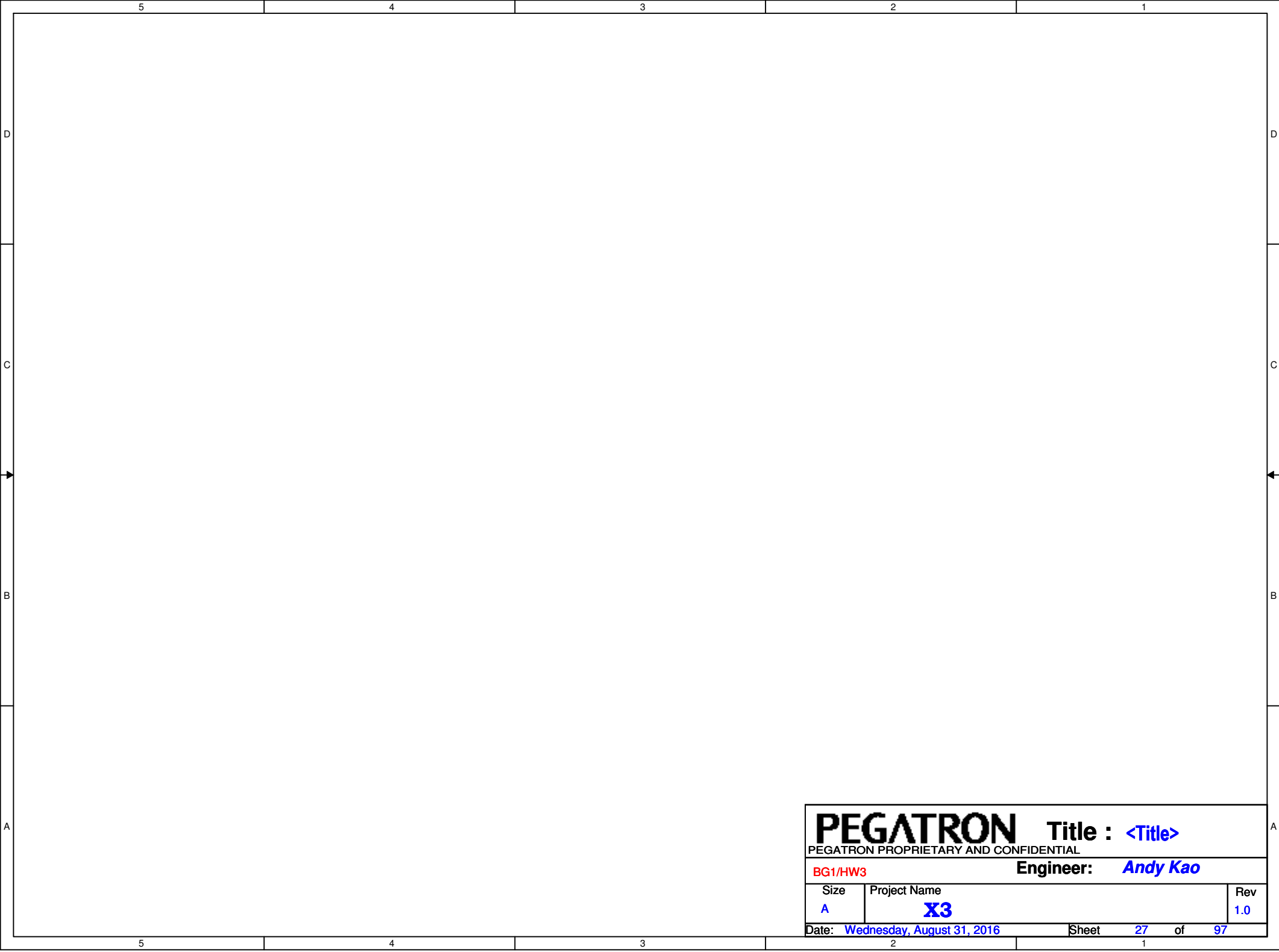
+3VSUS_ORG		+3VSUS_ORG	20,21,22,23,26
+VCC_RTC		+VCC_RTC	24,26,36,60
+VCCDSW		+VCCDSW	26,30
+VCCST_CPU		+VCCST_CPU	3,5,7,9,32
+3V		+3V	31,57,82,91
+3VSUS		+3VSUS	4,24,26,28,30,31,41,42,51,53,62,64,68,81,92



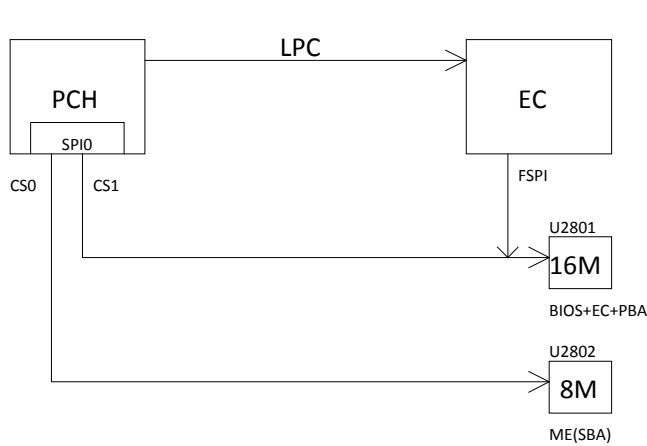
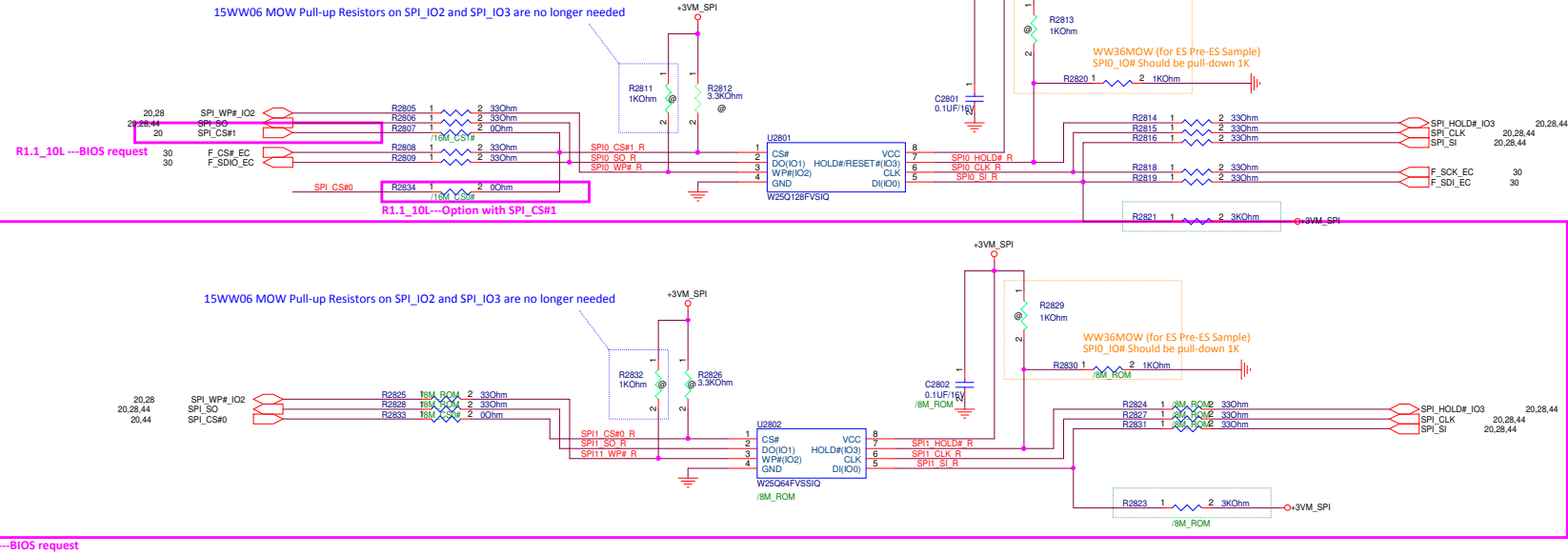
EC delay ALL\_SYSTEM\_PWRGD 2ms



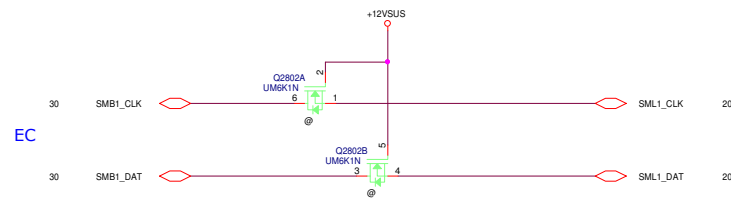




<b>PEGATRON</b> <b>Title :</b> <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>
Size <i>A</i>	Project Name <b>X3</b>	Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>27</i> of <i>97</i>

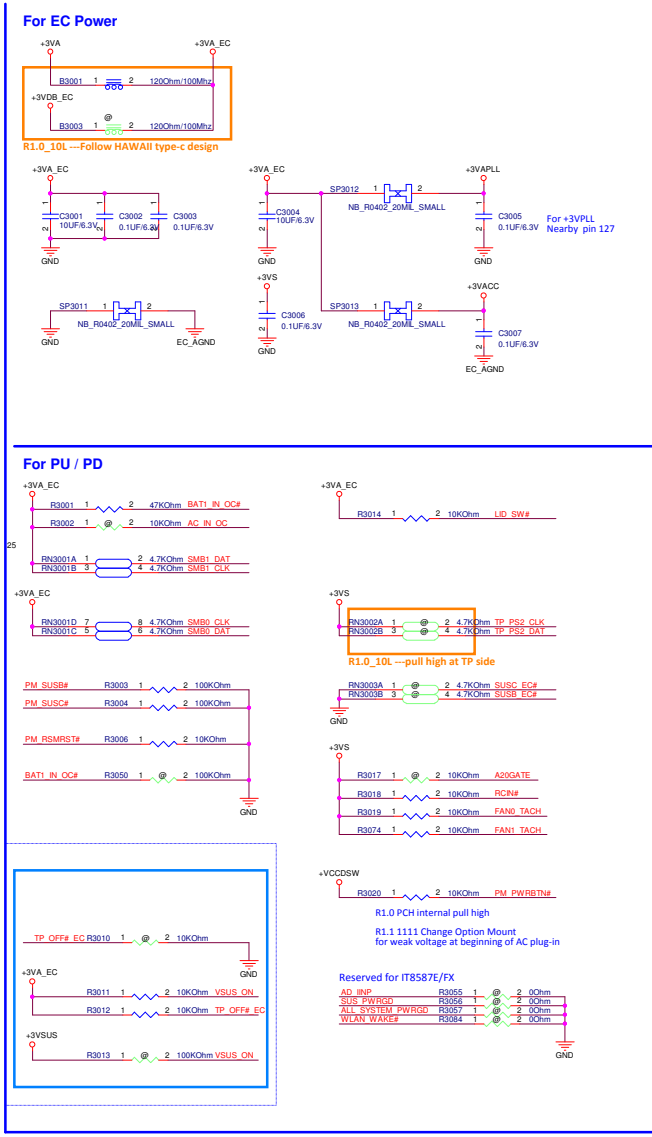
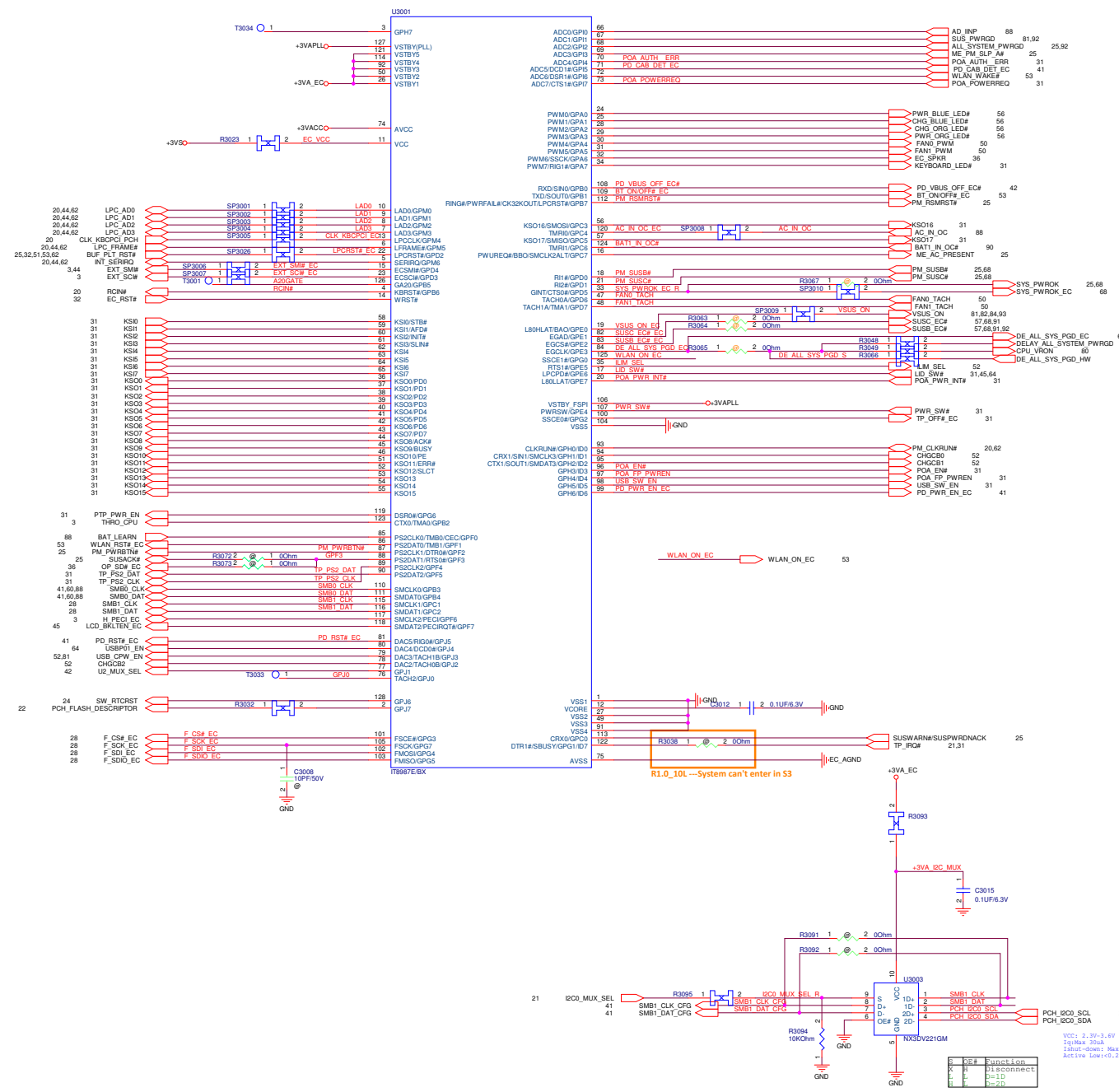


PCH SMBus

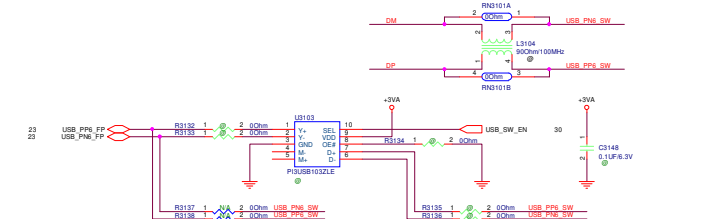
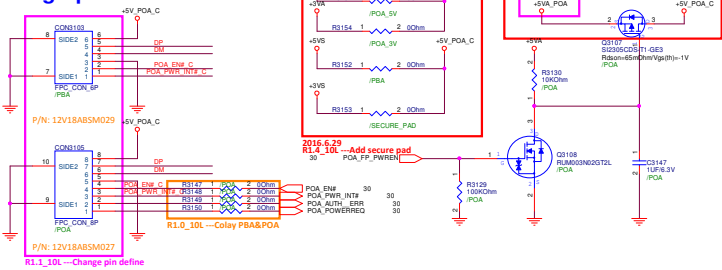


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										<table><tr><td colspan="10"><b>PEGATRON</b></td><td colspan="5">Title : <b>&lt;Title&gt;</b></td></tr><tr><td colspan="15">PEGATRON PROPRIETARY AND CONFIDENTIAL</td></tr><tr><td colspan="10"><b>BG1/HW3</b></td><td colspan="5">Engineer: <b>Andy Kao</b></td></tr><tr><td colspan="2">Size</td><td colspan="10">Project Name</td><td colspan="3">Rev</td></tr><tr><td colspan="2"><b>A</b></td><td colspan="10"><b>X3</b></td><td colspan="3"><b>1.0</b></td></tr><tr><td colspan="10">Date: <b>Wednesday, August 31, 2016</b></td><td colspan="5">Sheet <b>29</b> of <b>97</b></td></tr></table>															<b>PEGATRON</b>										Title : <b>&lt;Title&gt;</b>					PEGATRON PROPRIETARY AND CONFIDENTIAL															<b>BG1/HW3</b>										Engineer: <b>Andy Kao</b>					Size		Project Name										Rev			<b>A</b>		<b>X3</b>										<b>1.0</b>			Date: <b>Wednesday, August 31, 2016</b>										Sheet <b>29</b> of <b>97</b>				
<b>PEGATRON</b>										Title : <b>&lt;Title&gt;</b>																																																																																																								
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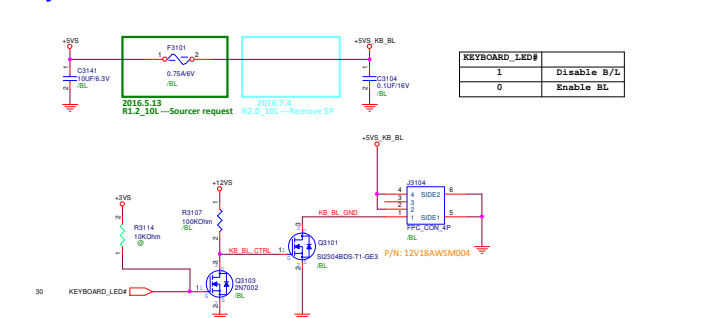
+3VA\_EC 28.32,44  
+3VS 3.4,21,22,23,24,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92  
+VBSUS 4.24,25,26,38,31,41,42,51,53,62,64,68,81,92  
+3VA 24,31,36,41,43,53,57,64,81,88,93  
+VCCDSW 25,26



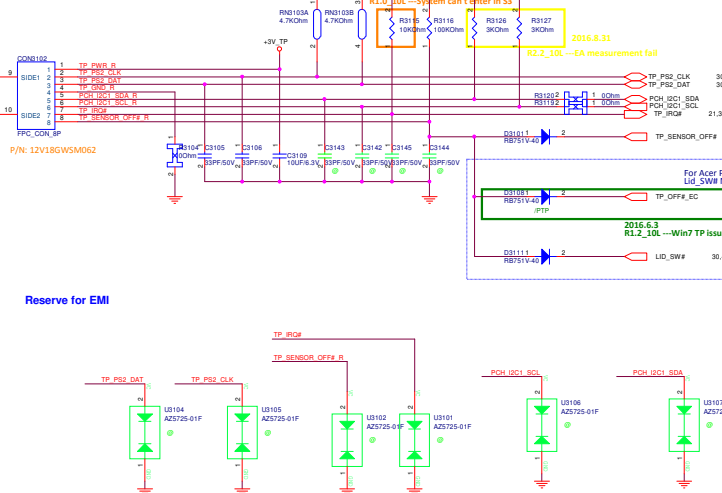
## Fingerprinter



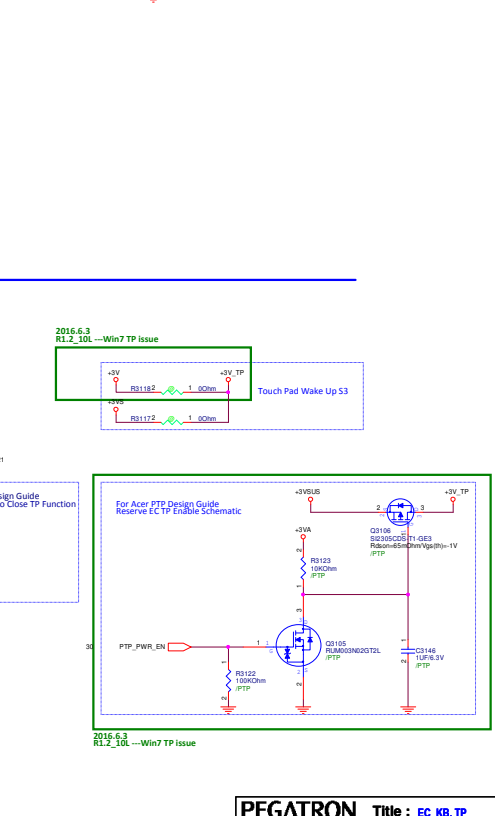
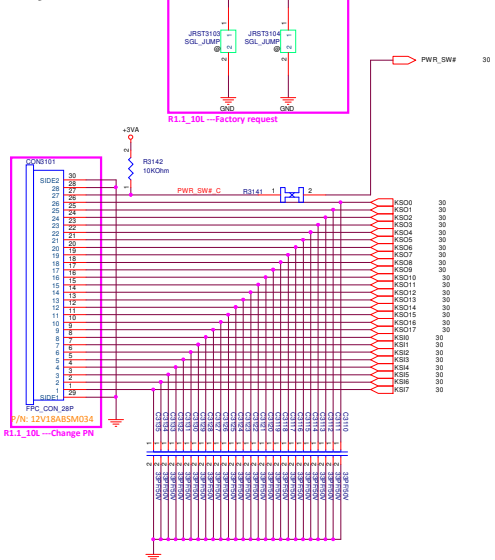
## Keyboard LED

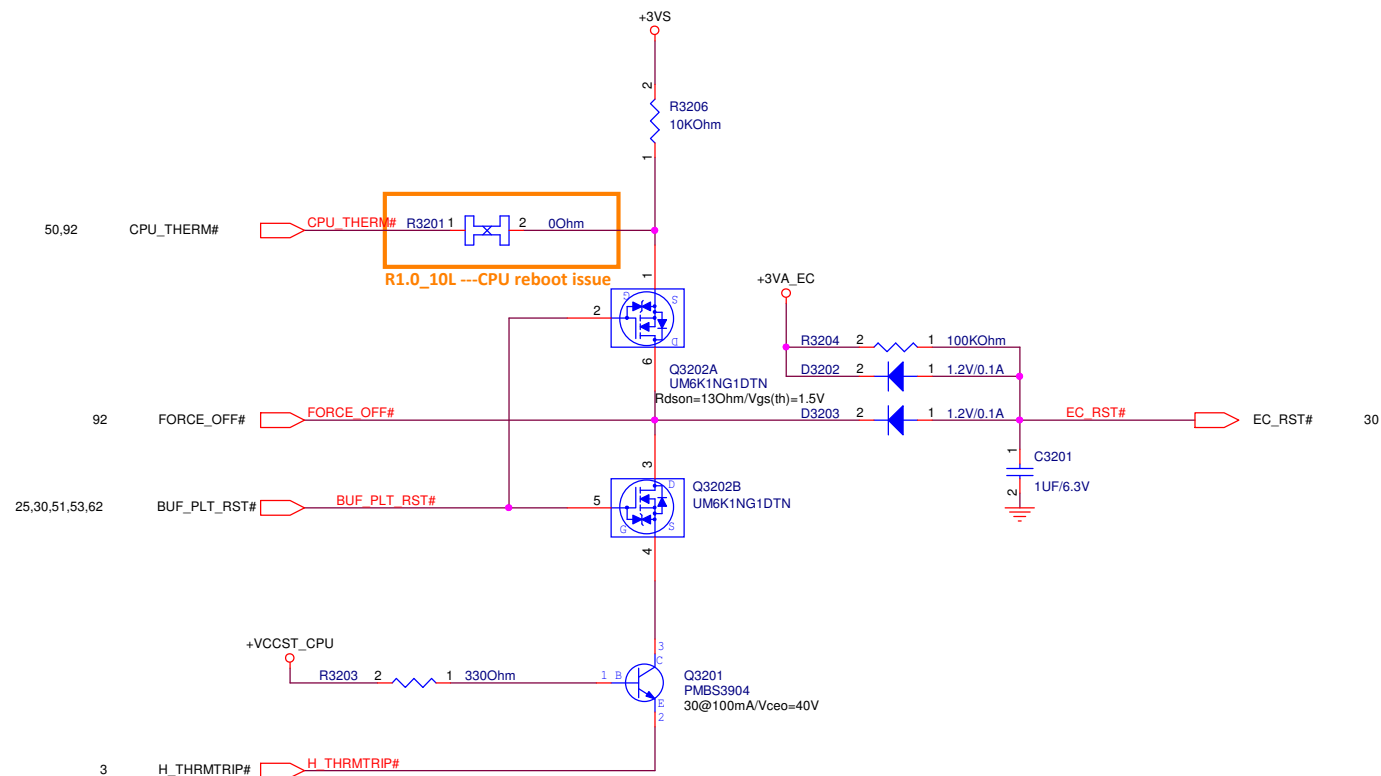


## Click Pad



## Keyboard

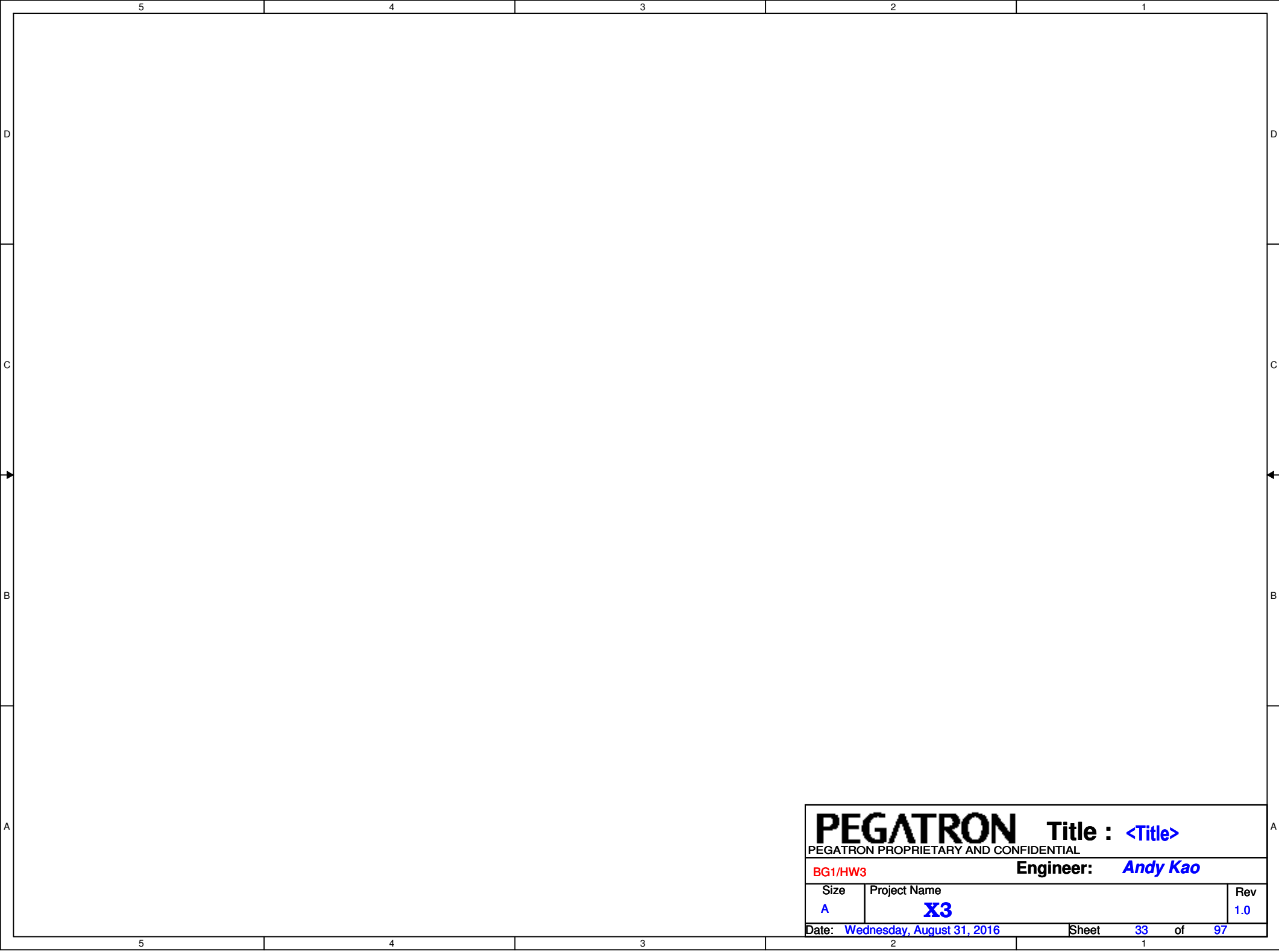




+VCCST\_CPU +VCCST\_CPU 3,5,7,9,25  
+3VA\_EC +3VA\_EC 28,30,44  
+3VS +3VS 3,4,21,22,23,24,30,31,36,37,44,45,47,50,51,53,57,62,64,91,92

<b>PEGATRON</b>		<b>Title :</b> RST_Reset Circuit	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		<b>Engineer:</b> Andy Kao	
Size B	Project Name <b>X3</b>	Rev 1.0	
Date: Wednesday, August 31, 2016		Sheet	32 of 97

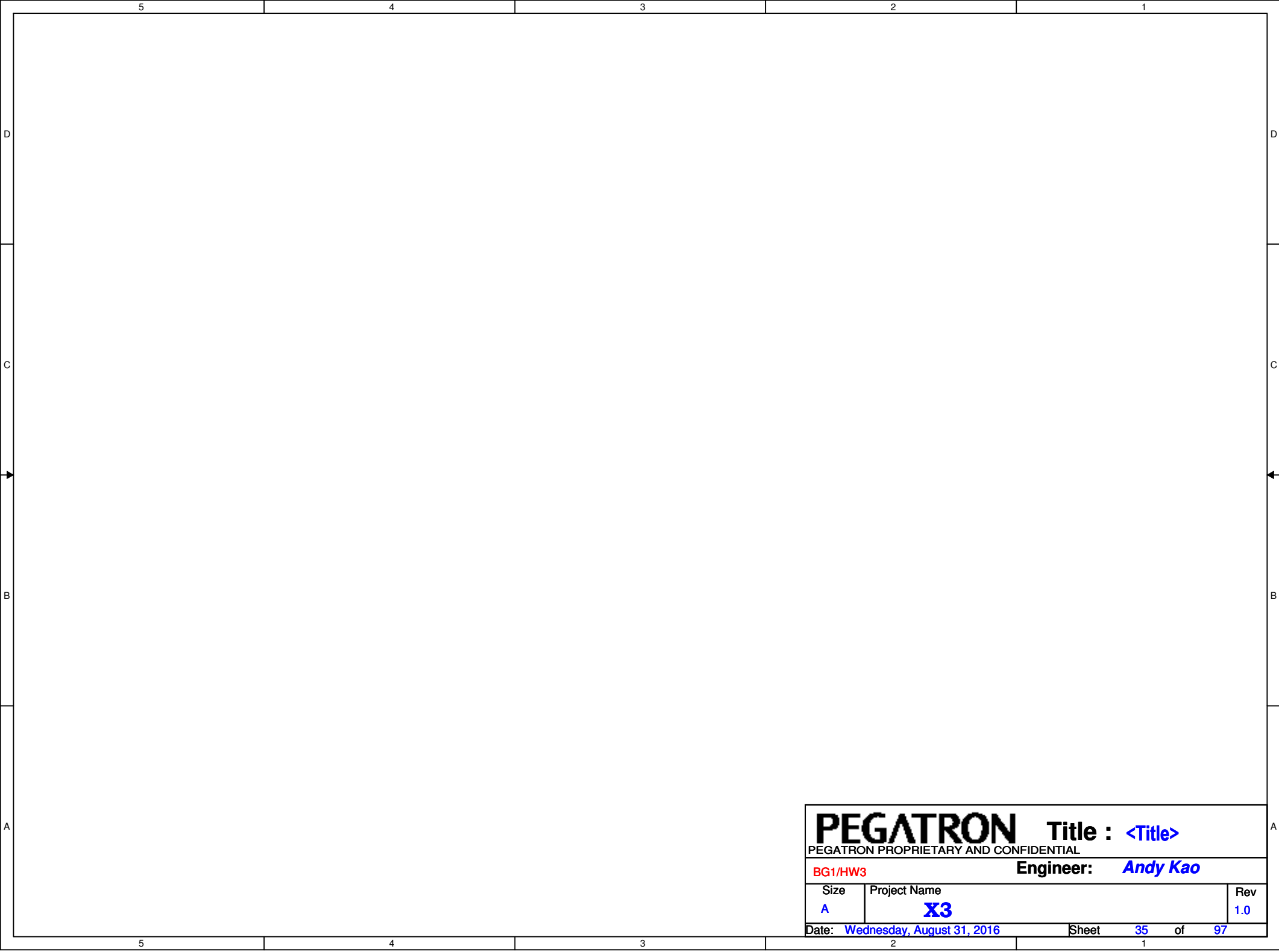




<b>PEGATRON</b> <b>Title :</b> <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>
Size <i>A</i>	Project Name <b>X3</b>	Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>33</i> of <i>97</i>

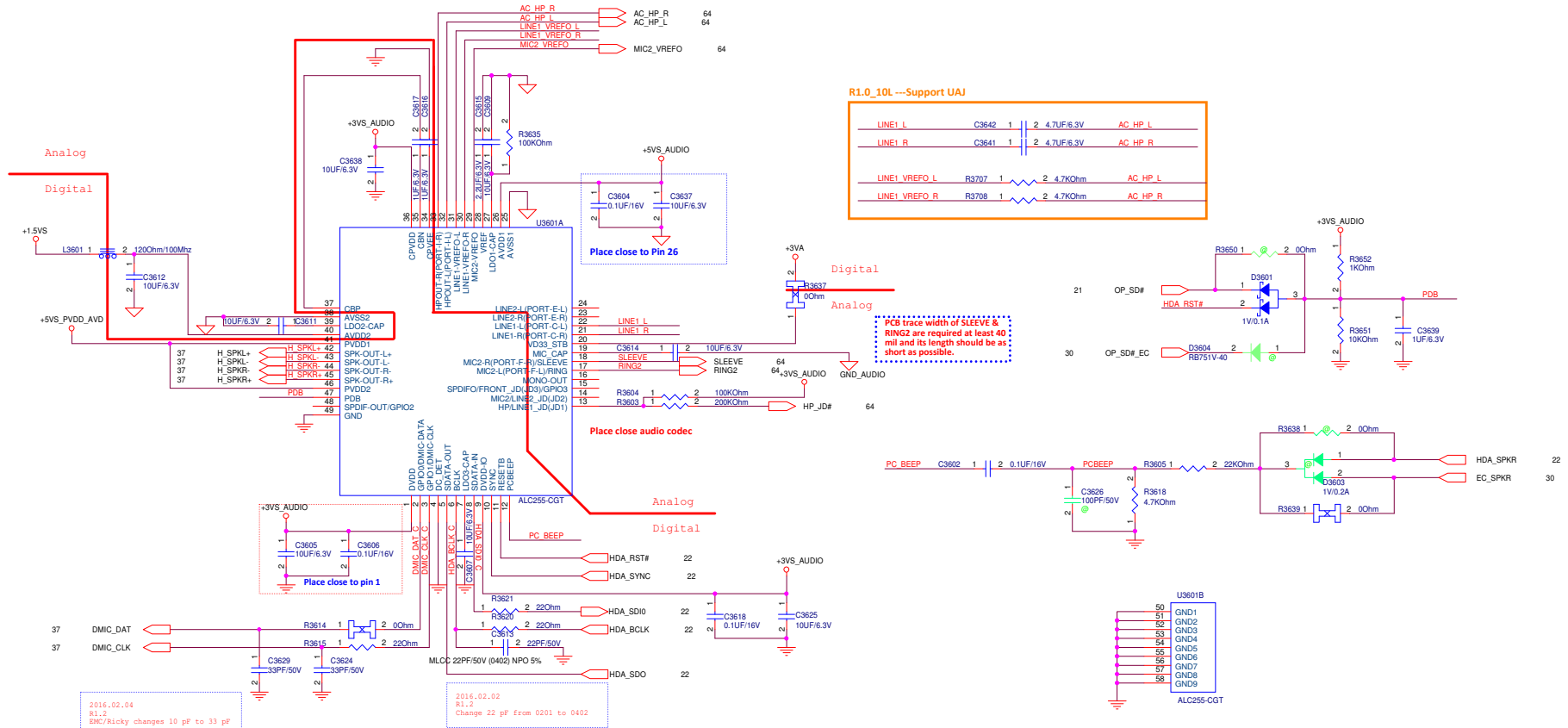
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D					D
C					C
B					B
A					A

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<div>BG1/HW3</div>		<div>Engineer: Andy Kao</div>
<div>Size</div> <div>A</div>	<div>Project Name</div> <div>X3</div>	<div>Rev</div> <div>1.0</div>
<div>Date: Wednesday, August 31, 2016</div>		<div>Sheet 34 of 97</div>



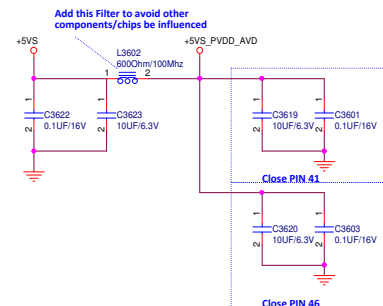
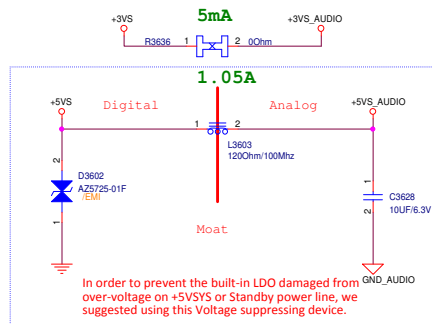
<b>PEGATRON</b> <b>Title :</b> <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>
Size <i>A</i>	Project Name <b>X3</b>	Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>35</i> of <i>97</i>

+1.5VS +1.5VS 47.57.85  
 +3VS +3VS 3.4,21,22,23,24,30,31,32,37,44,45,47,50,51,53,57,62,64,91,92  
 +5VS +5VS 31,45,48,50,51,57,80,91



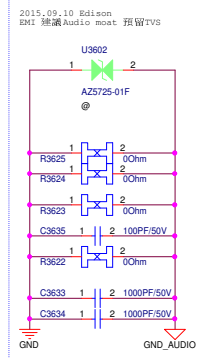
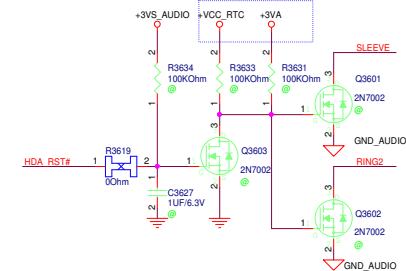
2016.02.04  
 R1.2  
 BAC/Ricky changes 10 pF to 33 pF

2016.02.02  
 R1.2  
 Change 22 pF from 0201 to 0402

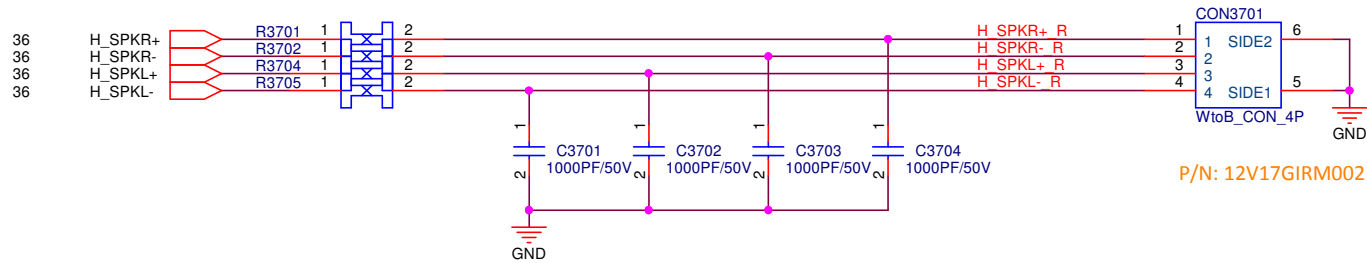


<<Attention>>  
 For power\_on/off de-pop circuit and system booting warning signal: Please System BIOS Engineer Note :  
 1. If you want the system make warning signal after power on, please let EC\_MUTE# High.  
 2. If your design want to system make warning signal, for example No CPU or Memory installation or Bad BIOS, please change to OR Gate or contact our local FAEs for more details about the control circuit

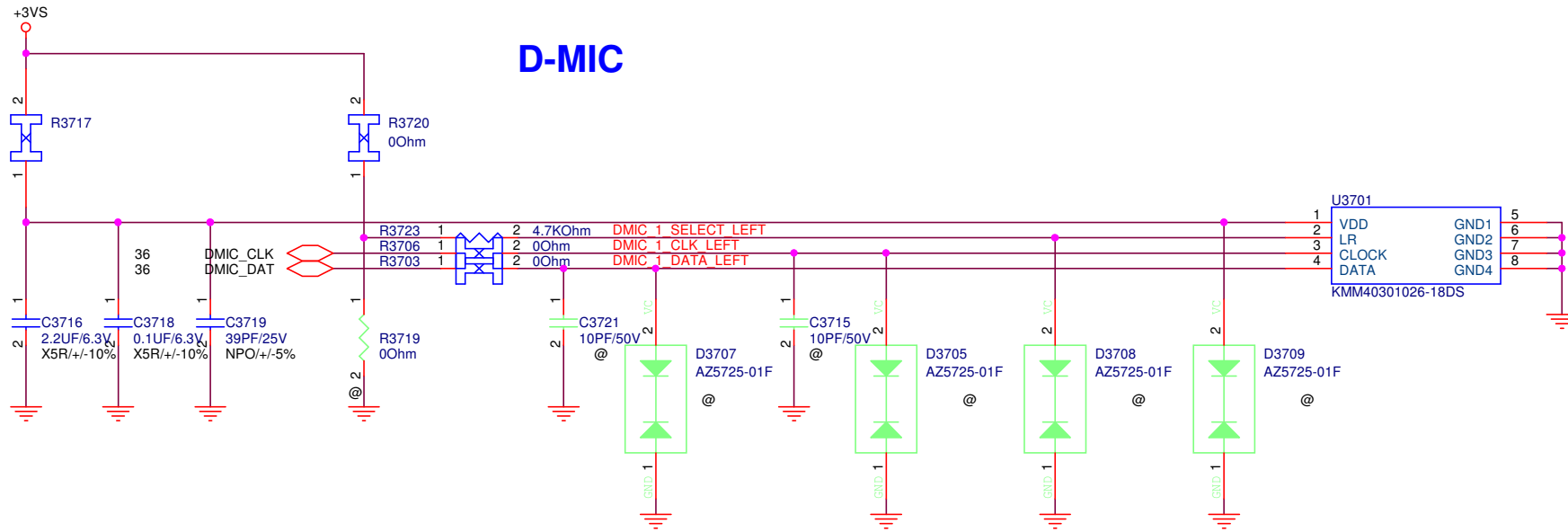
#### Grounding circuit for combo jack SLEEVE pin



# Speaker



# D-MIC



D

C |

B

A

**PEGATRON** Title : <Title>

**PEGATRON PROPRIETARY AND CONFIDENTIAL**

BG1/HW3

**Engineer:** *Andy Kao*

---

Size

A

Project Name
--------------

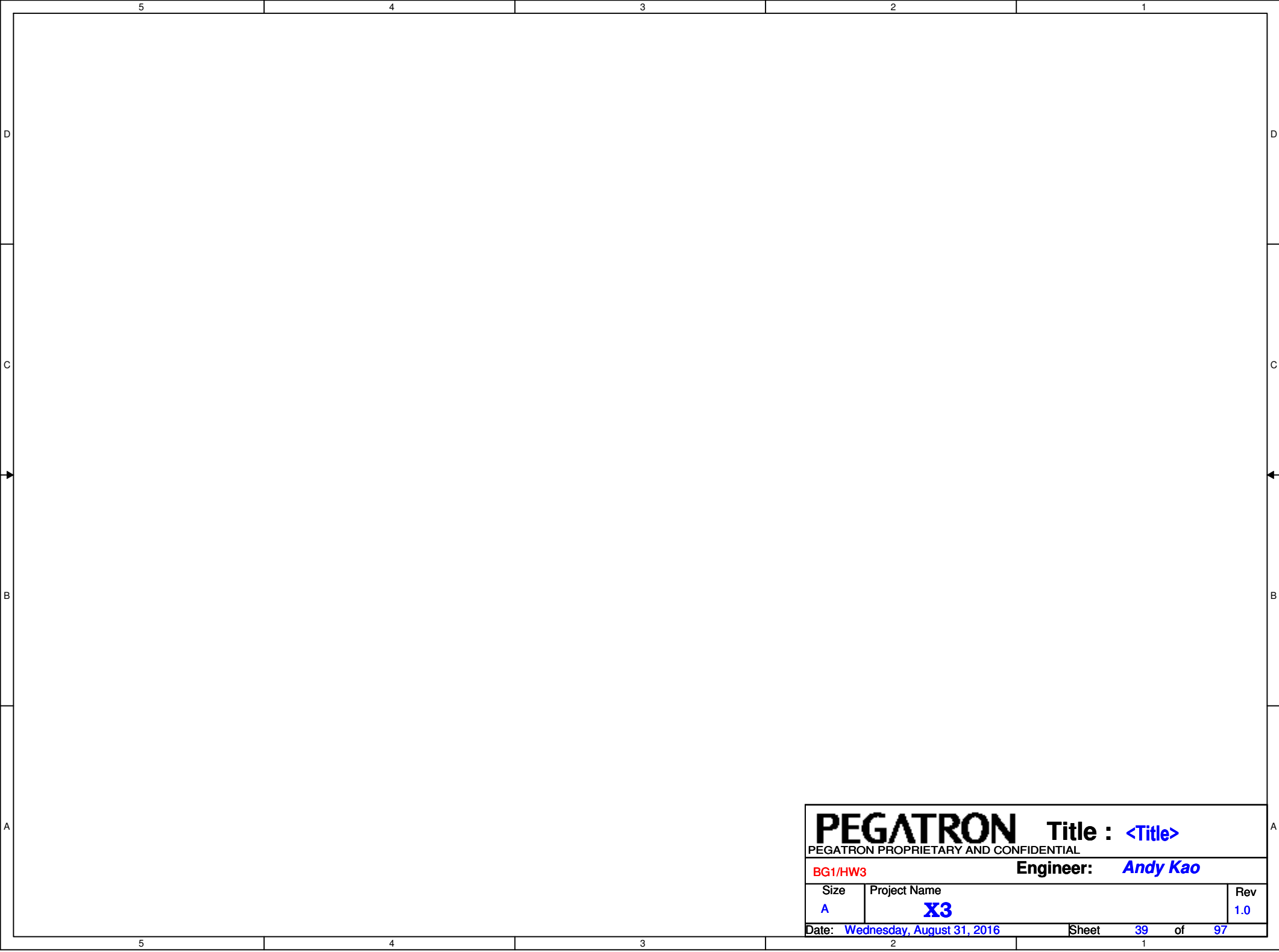
### X3

Rev

1.0

Date: Wednesday, August 31, 2016

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PEGATRON

Title : <Title>

PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1/HW3

Engineer: Andy Kao

Size	Project Name	Rev
A	X3	1.0

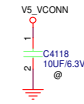
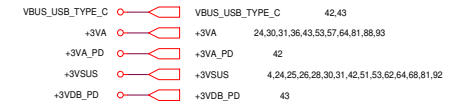
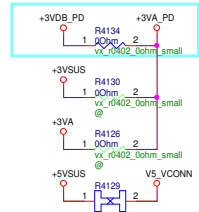
Date: Wednesday, August 31, 2016

Sheet 39 of 97

	5	4	3	2	1
D					D
C					C
B					B
A					A

<div> <div>PEGATRON</div> <div>PEGATRON PROPRIETARY AND CONFIDENTIAL</div> </div>			<div> <div>Title : &lt;Title&gt;</div> </div>		
<div> <div>BG1/HW3</div> </div>			<div> <div>Engineer:</div> <div>Andy Kao</div> </div>		
<div> <div>Size</div> <div>A</div> </div>	<div> <div>Project Name</div> <div>X3</div> </div>				<div> <div>Rev</div> <div>1.0</div> </div>
<div> <div>Date:</div> <div>Wednesday, August 31, 2016</div> </div>			<div> <div>Sheet</div> <div>40</div> </div>	<div> <div>of</div> <div>97</div> </div>	

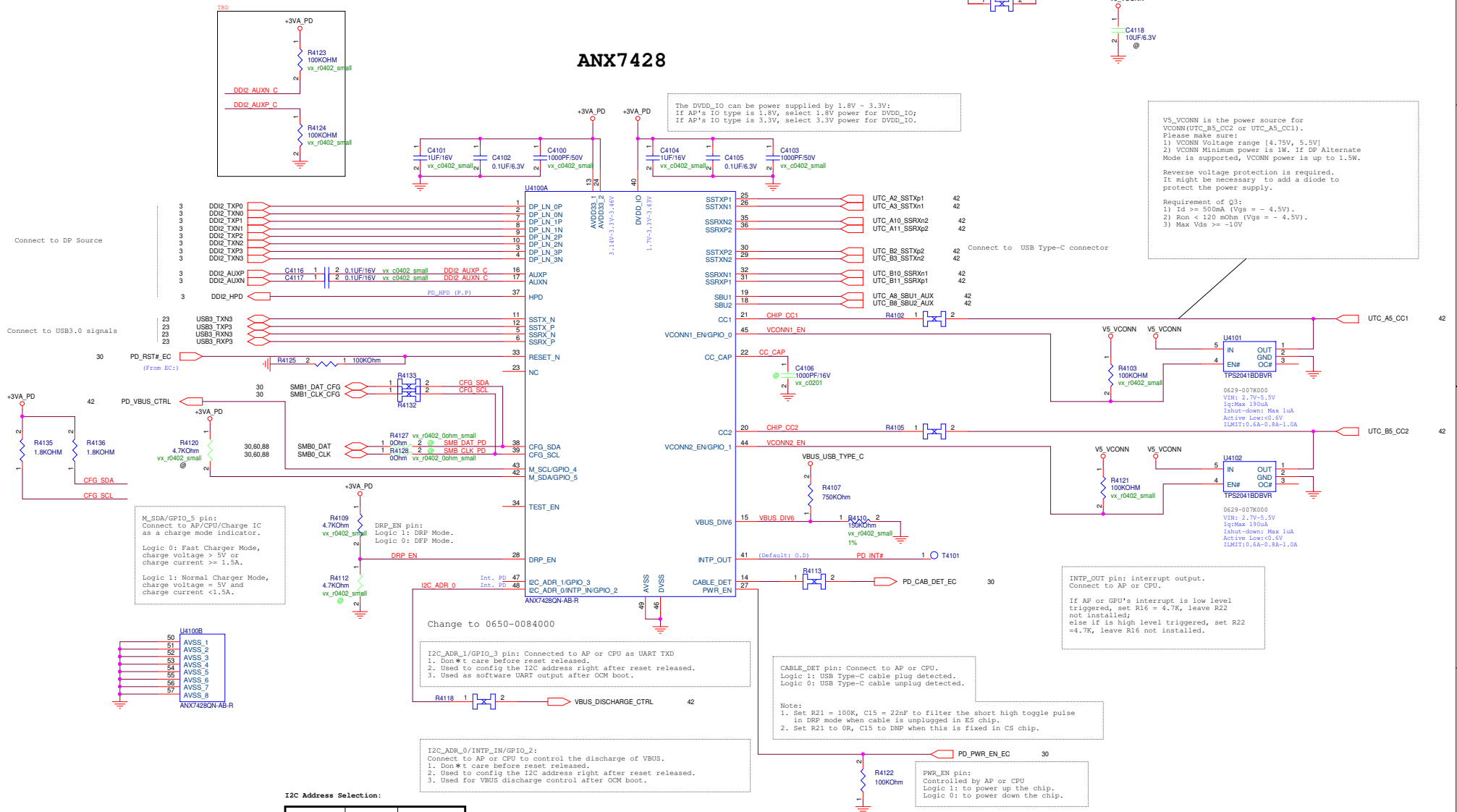




V5\_VCONN is the power source for VCONN(UTC\_B5\_CC2 or UTC\_A5\_CC1). Please make sure:

- 1) VCONN Voltage range [4.75V, 5.5V]
- 2) VCONN Minimum power is 1W. If DP Alternate Mode is supported, VCONN power is up to 1.5W.

Reverse voltage protection is required. It might be necessary to add a diode to protect the power supply.



I2C_ADR_1	I2C_ADR_0	I2C Address
Logic 0	Logic 0	0x50
Logic 0	Logic 1	0x72
Logic 1	Logic 0	0x7c
Logic 1	Logic 1	0x80

1. The I2C address is determined approximately 500ns after RESET\_N turns from 0 to 1, these two pins' input should be kept at a stable value during this period.
2. There are internal pull-down resistors on I2C\_ADR\_0 and I2C\_ADR\_1 pins.
3. If external pull-up resistor is not populated, the I2C\_ADR\_0 or I2C\_ADR\_1 is logic 0.
4. If external pull-up is populated, the I2C\_ADR\_0 or I2C\_ADR\_1 is logic 1.

<Variant Name>

PEGATRON Title : POWER\_FLOWCHART

**Engineer:** **Andy Kao**

Size C	Project Name <b>X3</b>	Rev 1.0
Date: <u>Wednesday, August 31, 2016</u> Sheet <u>41</u> of <u>97</u>		



## Hardware Solution For Dead Battery

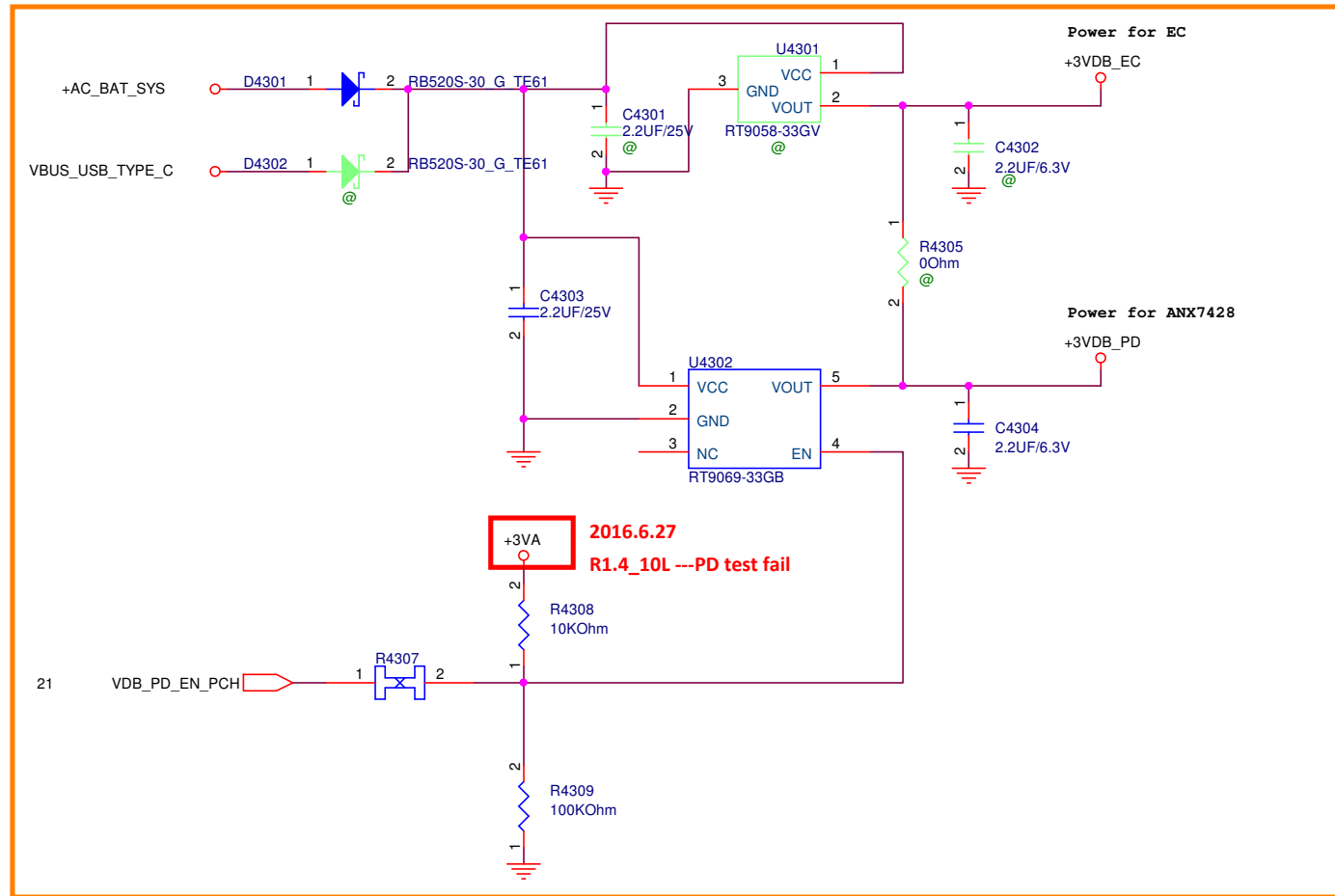
For notebook applications, if the battery charger needs higher voltage than 5V to operate correctly, execute the steps below in the order they are listed:

VBUS_USB_TYPE_C		VBUS_USB_TYPE_C	41,42
+AC_BAT_SYS		+AC_BAT_SYS	45,80,81,82,83,88
+3VDB_EC		+3VDB_EC	30
+3VDB_PD		+3VDB_PD	41

Requirement of U1:

- 1) Vin range: 4V-30V.
- 2) Vout: EC's operating voltage + Vf of D1
- 3) Output current >= EC's operating current.

### R1.0\_10L ---Follow HAWAll type-c design



**2016.6.27**  
**R1.4\_10L ---PD test fail**

<Variant Name>

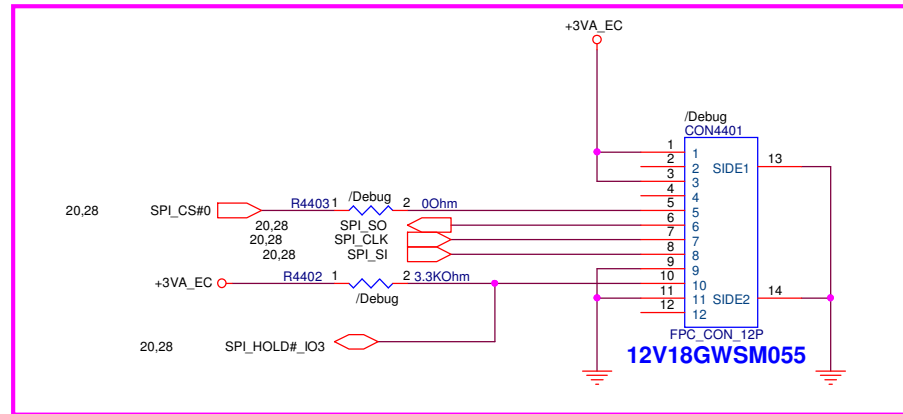
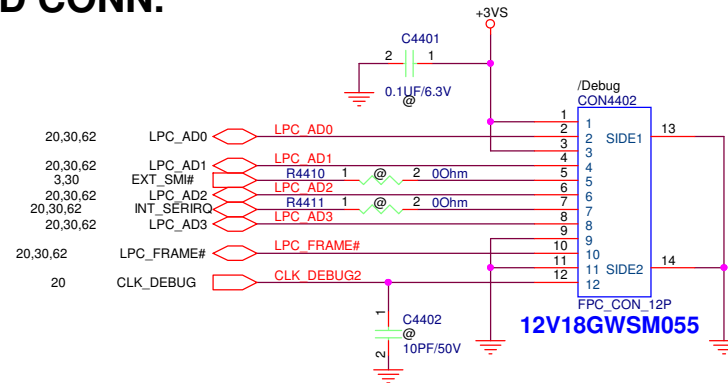
**PEGATRON** Title : **Dead Battery**  
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: **Andy Kao**

Size Custom	Project Name <b>X3</b>	Rev 1.0
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Date: **Wednesday, August 31, 2016** Sheet **43** of **97**

# DEBUG CARD CONN.

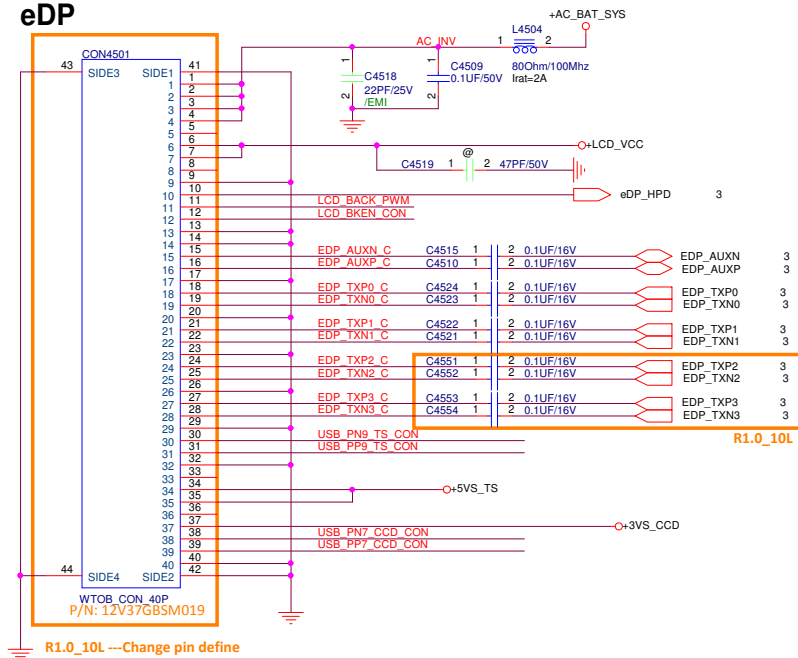


R1.1\_10L ---BIOS request

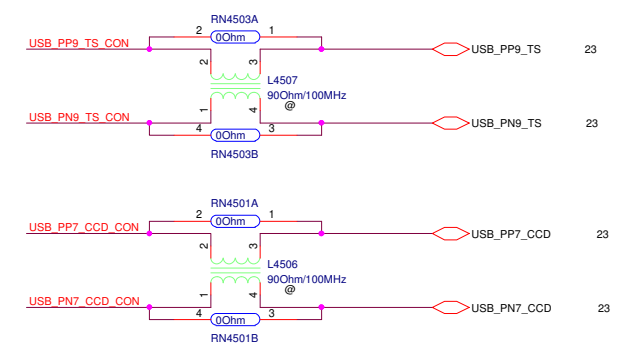
<Variant Name>

<b>PEGATRON</b>		<b>Title :</b> <b>DEBUG CONN.</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		<b>Engineer:</b> <b>Andy Kao</b>	
Size <b>B</b>	Project Name <b>X3</b>		Rev <b>1.0</b>
Date: <b>Wednesday, August 31, 2016</b>		Sheet <b>44</b> of <b>97</b>	

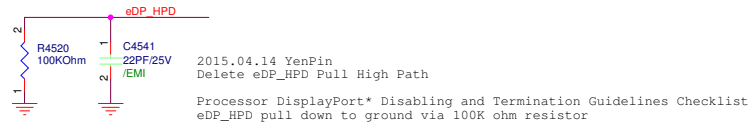
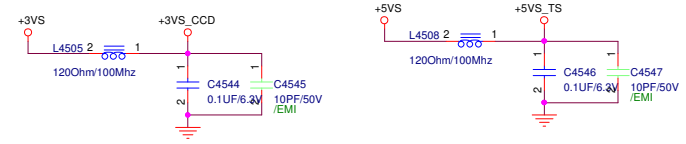
# eDP



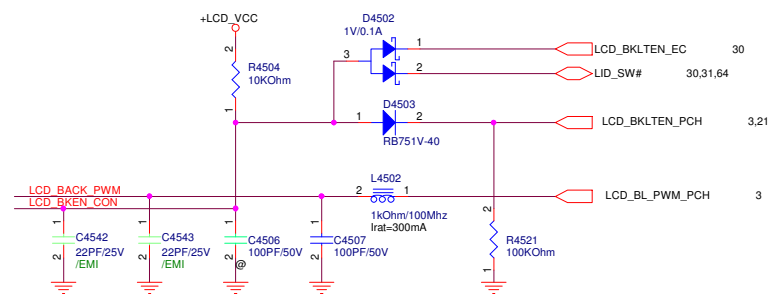
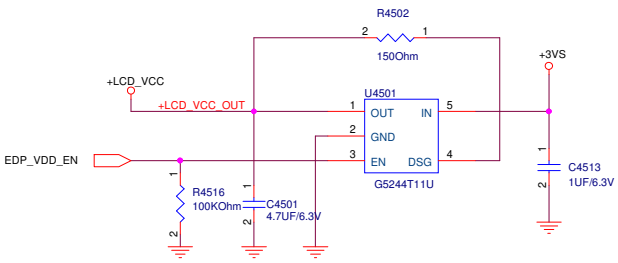
+3VS	+3VS	3,4,21,22,23,24,30,31,32,36,37,44,47,50,51,53,57,62,64,91,92
+5VS	+5VS	31,36,48,50,51,57,80,91
+AC_BAT_SYS	+AC_BAT_SYS	43,80,81,82,83,88



## Camera



## LCD VDDEN / +LED\_VCC



<Variant Name>		Title : eDP CONN	
Size	Project Name	Engineer:	Andy Kao
Custom	X3	Rev	1.0
Date:	Wednesday, August 31, 2016	Sheet	45 of 97



<b>PEGATRON</b>		Title : <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: <i>Andy Kao</i>	
Size A	Project Name <b>X3</b>		Rev 1.0
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>46</i> of <i>97</i>	

T4702 1 PRE

Output pre-emphasis setting; Internal pull down at ~150k $\Omega$ , 3.3V I/O.  
L: no pre-emphasis  
M: 1.6dB pre-emphasis  
M: 2.5dB pre-emphasis

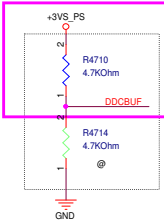
T4701 1 EQ

Receiver equalization setting; Internal pull down at ~150k $\Omega$ , 3.3V I/O.  
L: programmable EQ for channel loss up to 12.6dB  
M: programmable EQ for channel loss up to 4.3dB  
M: programmable EQ for channel loss up to 8.6dB

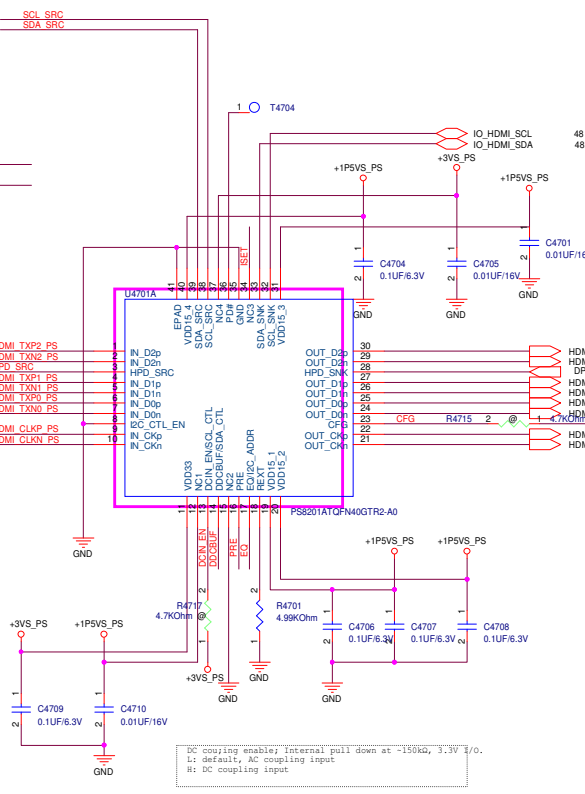
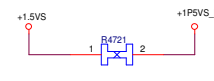
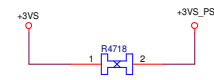
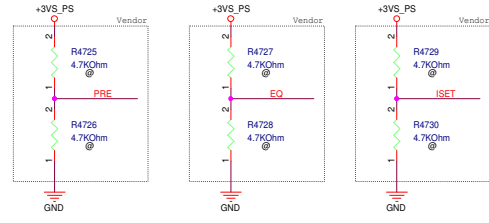
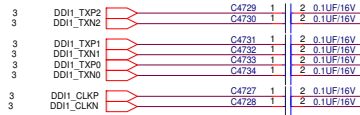
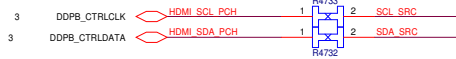
T4703 1 ISET

TMDS output swing adjustment; Internal pull down at ~150k $\Omega$ , 3.3V I/O.  
L: default  
M: increase +13%  
M: reduce -13%

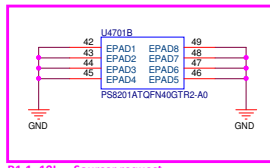
R1.1\_10L ---Follow megatron



Enable active DDC buffer; Internal pull down at ~150k $\Omega$ , 3.3V I/O.  
L: default, passive DDC pass-through  
M: active DDC buffer with default threshold  
M: active DDC buffer without internal pull up resistor



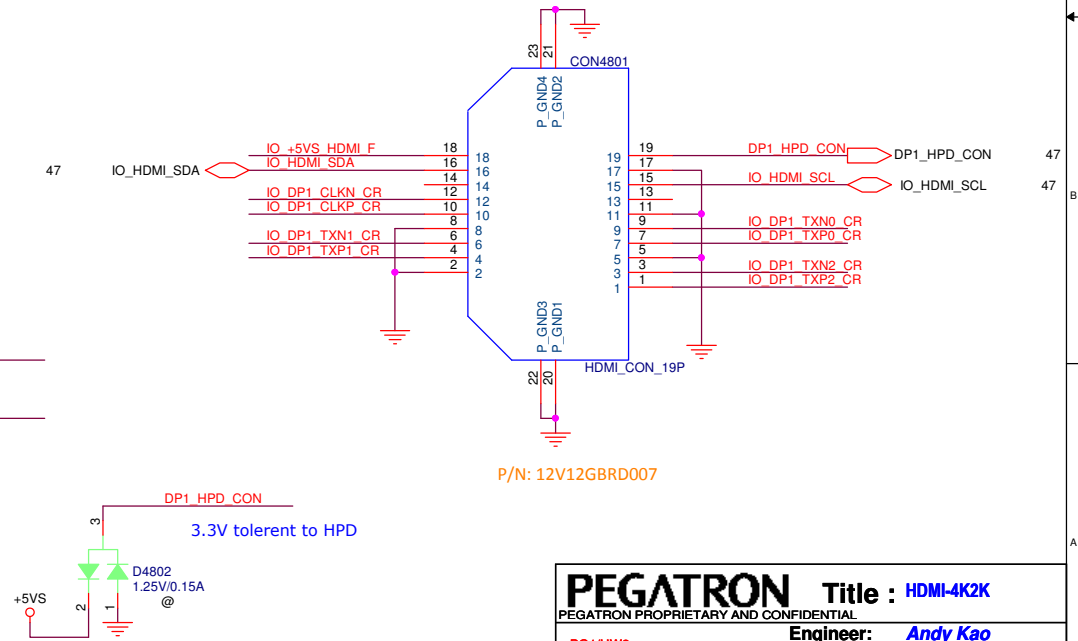
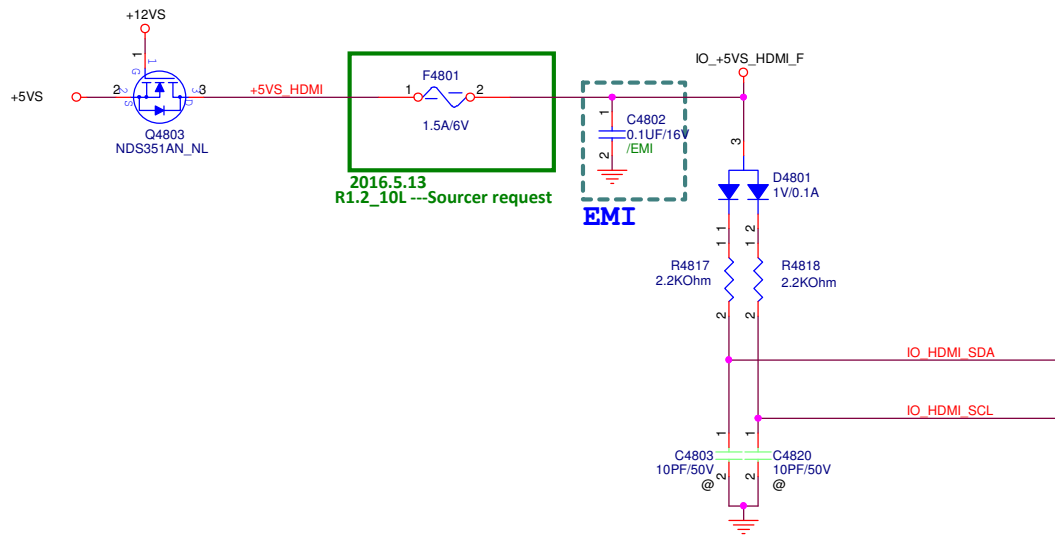
Configuration pin, 3.3V I/O, internal pull down at ~150k $\Omega$ , 3.3V I/O.  
L: HDMI ID disable  
M: HDMI ID enable  
(Typ:1.5V; Max:1.53V; Min:1.47V)



R1.1\_10L ---Sourcer request

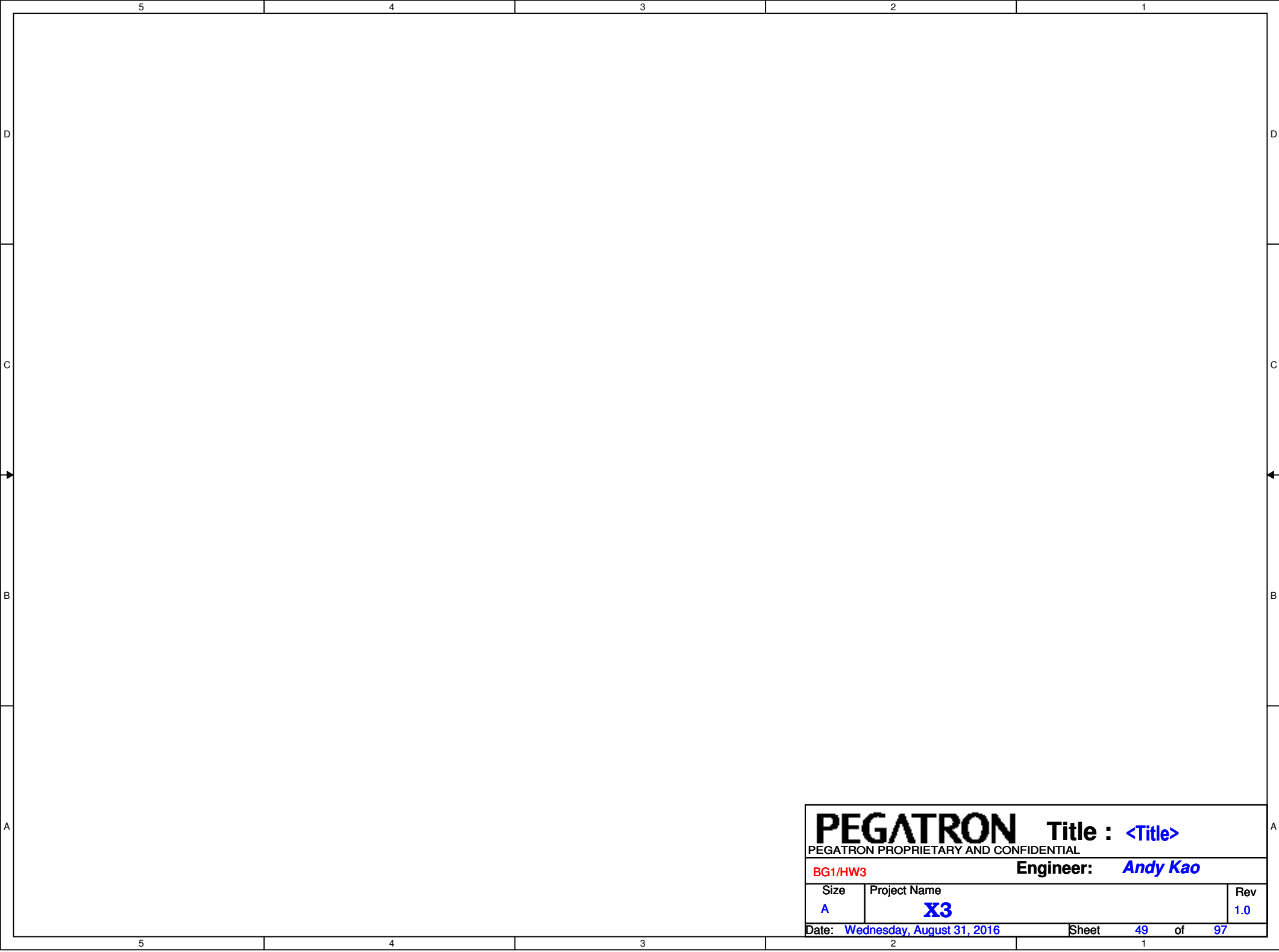
DC coupling enable; Internal pull down at ~150k $\Omega$ , 3.3V I/O.  
L: default, AC coupling input  
M: DC coupling input

## HDMI



<b>PEGATRON</b>		<b>Title :</b> HDMI-4K2K	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		<b>Engineer:</b> Andy Kao	
Size B	Project Name <b>X3</b>		Rev 1.0
Date: Wednesday, August 31, 2016		Sheet 48	of 97



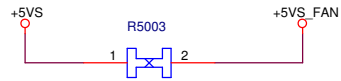
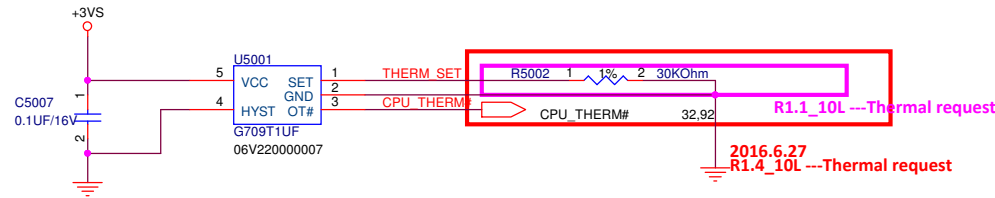


<b>PEGATRON</b> <b>Title :</b> <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>
Size <i>A</i>	Project Name <b>X3</b>	Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>49</i> of <i>97</i>

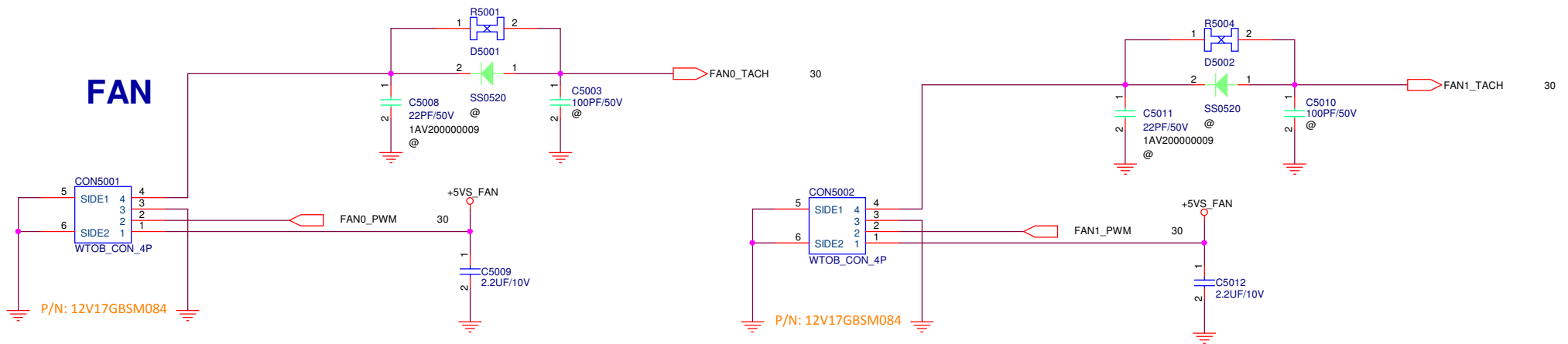
# Thermal Sensor

temp setting : 80 degree

$RSET(k\Omega) = 0.0012T^{\circ}T - 0.9308T + 96.147$



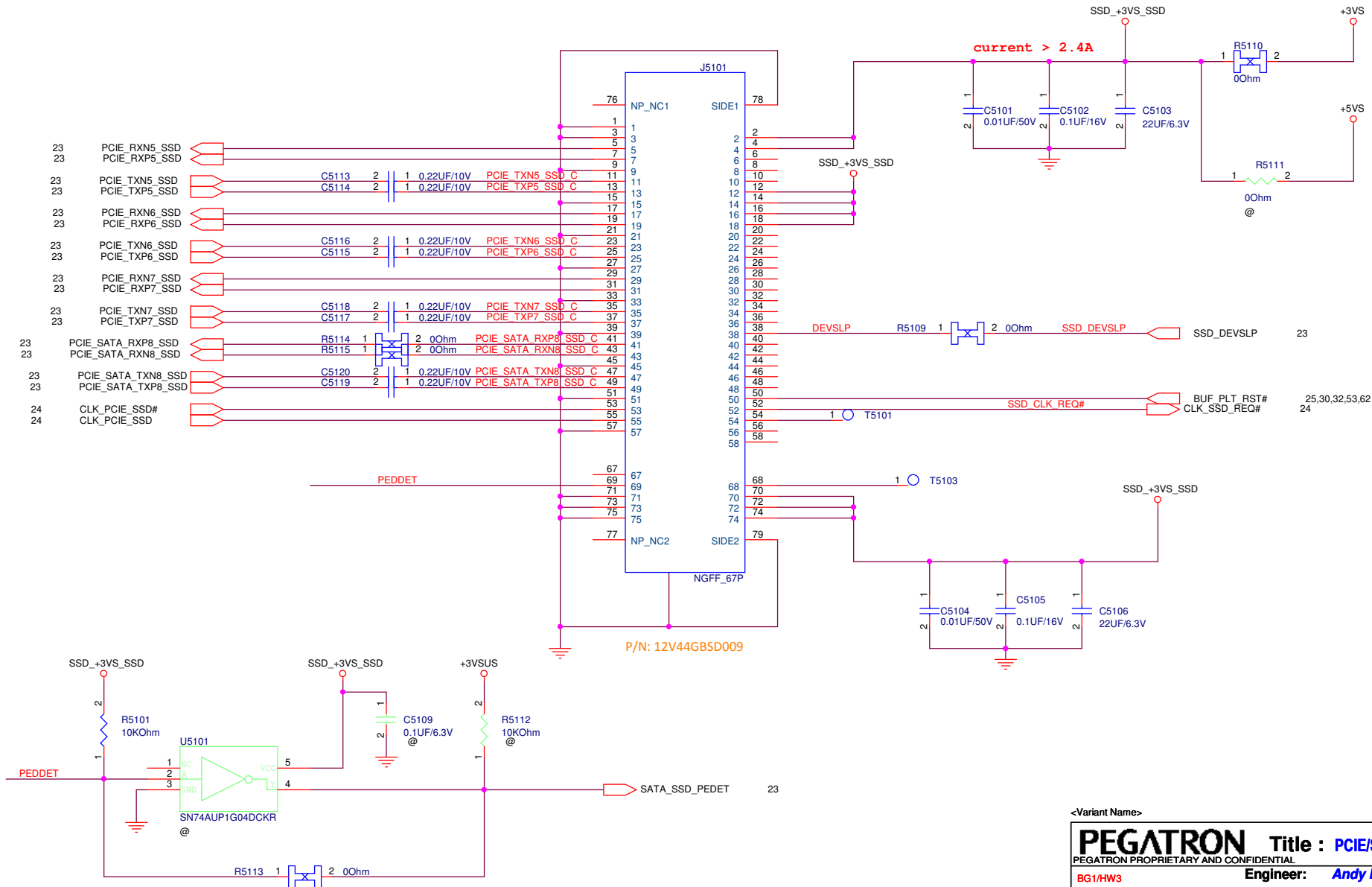
## FAN



<Variant Name>

<b>PEGATRON</b>		Title : Thermal/Fan	
BG1/HW3		Engineer: Andy Kao	
Size B	Project Name X3	Rev 1.0	
Date: Wednesday, August 31, 2016		Sheet 50 of 97	

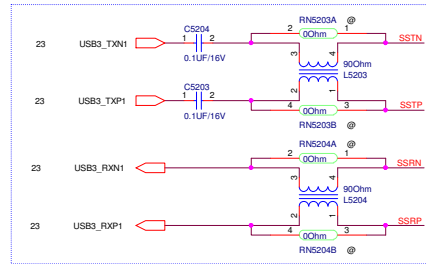
SSD(SATA/PCIE x4) NGFF socket (M-key)



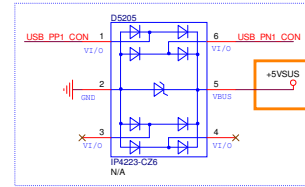
<Variant Name>			
<b>PEGATRON</b>		<b>Title : PCIE/SATA SSD</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		<b>Engineer: Andy Kao</b>	
Size	Project Name		Rev
Custom	<b>X3</b>		1.0
Date: <b>Wednesday, August 31, 2016</b>		Sheet	51 of 97

## USB 3.0

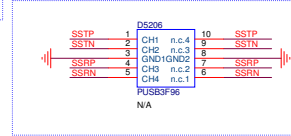
### USB3.0 Choke



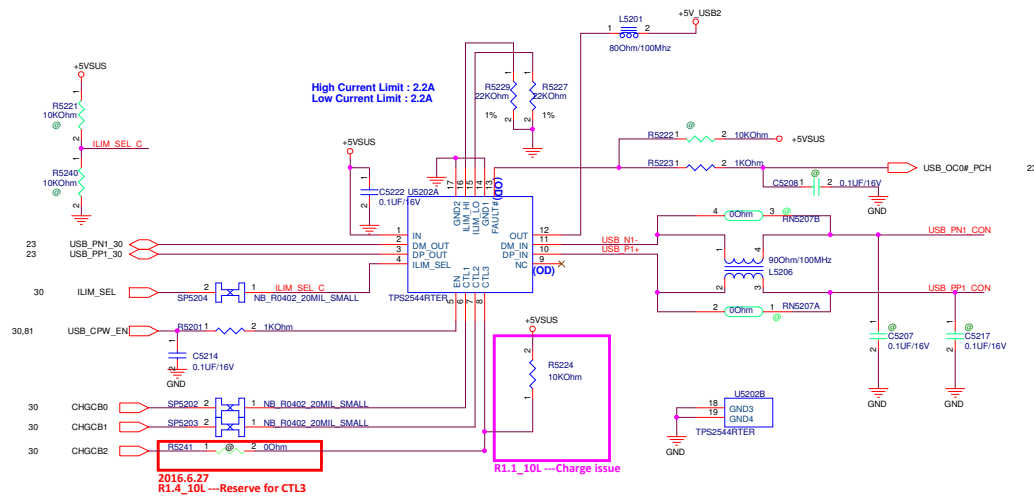
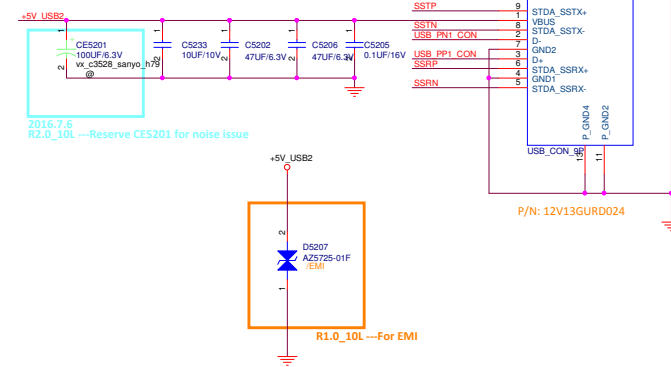
### USB2.0 ESD



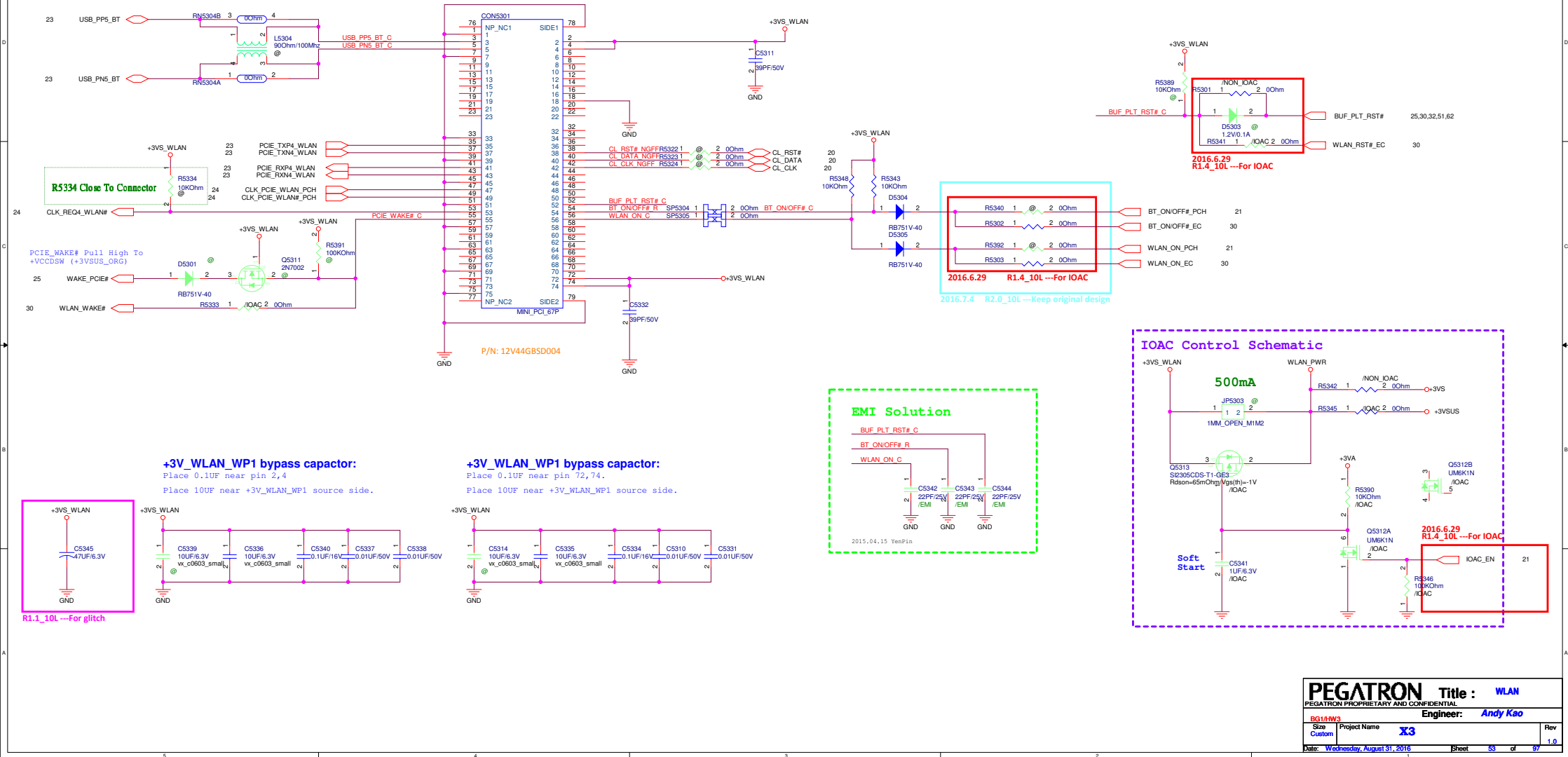
### USB3.0 ESD



## USB 3.0 - Type A



# WLAN/BT with NGFF socket E



D

C

B

A

**PEGATRON** Title : **USB HUB**

**PEGATRON PROPRIETARY AND CONFIDENTIAL**

<OrgName>

**Engineer:** *Andy Kao*

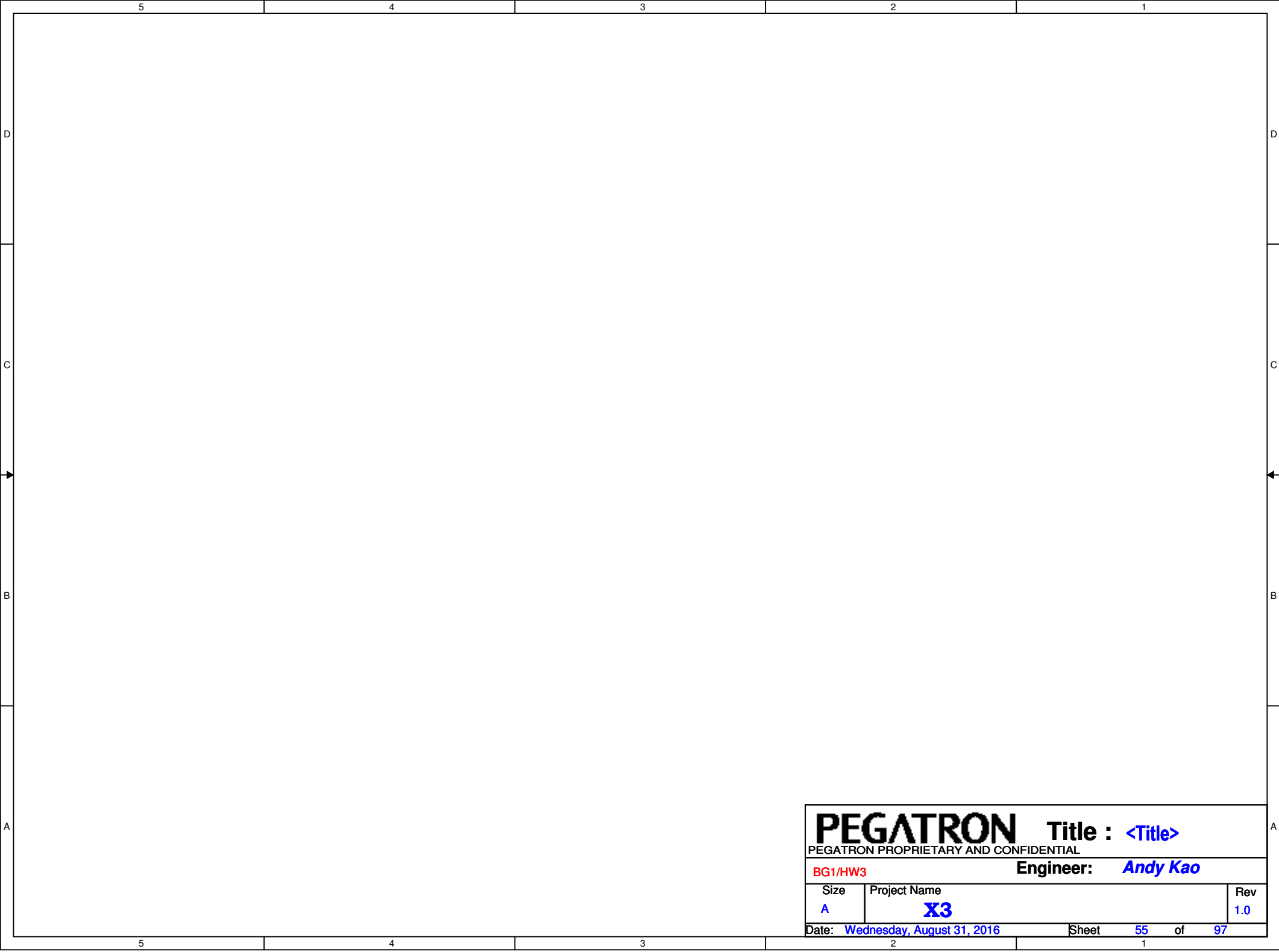
Size  
A

Project Name	<b>X3</b>
--------------	-----------

Rev	
1.0	

Date: Wednesday, August 31, 2016

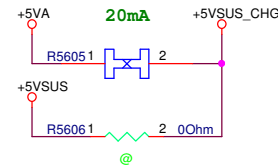
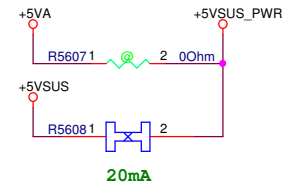
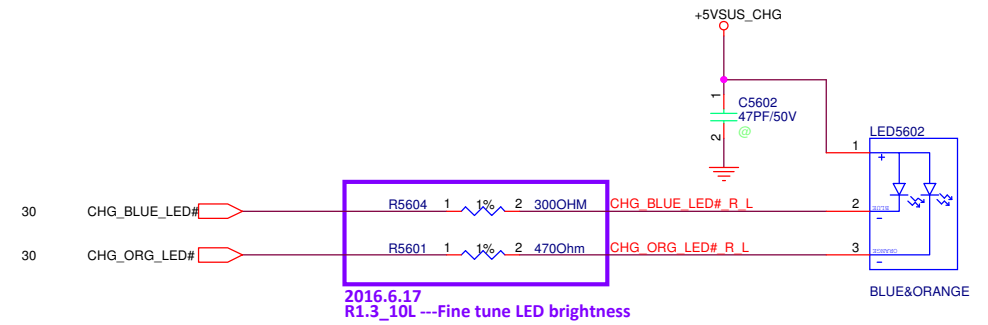
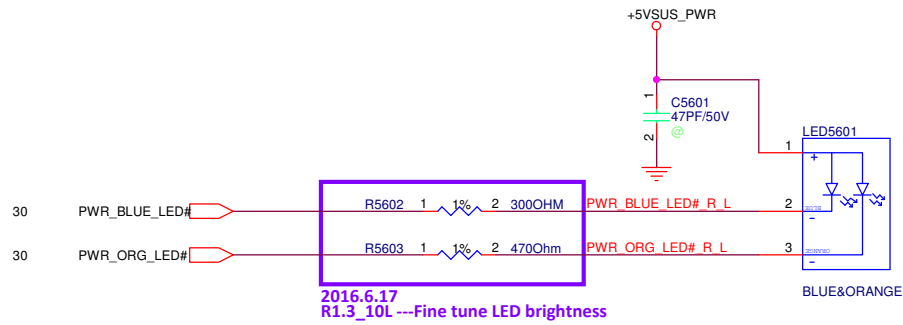
Sheet 54 of 97



<b>PEGATRON</b>		<b>Title :</b> <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>	
Size <i>A</i>	Project Name <i>X3</i>		Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>55</i> of <i>97</i>	

## POWER LED

## Charger LED

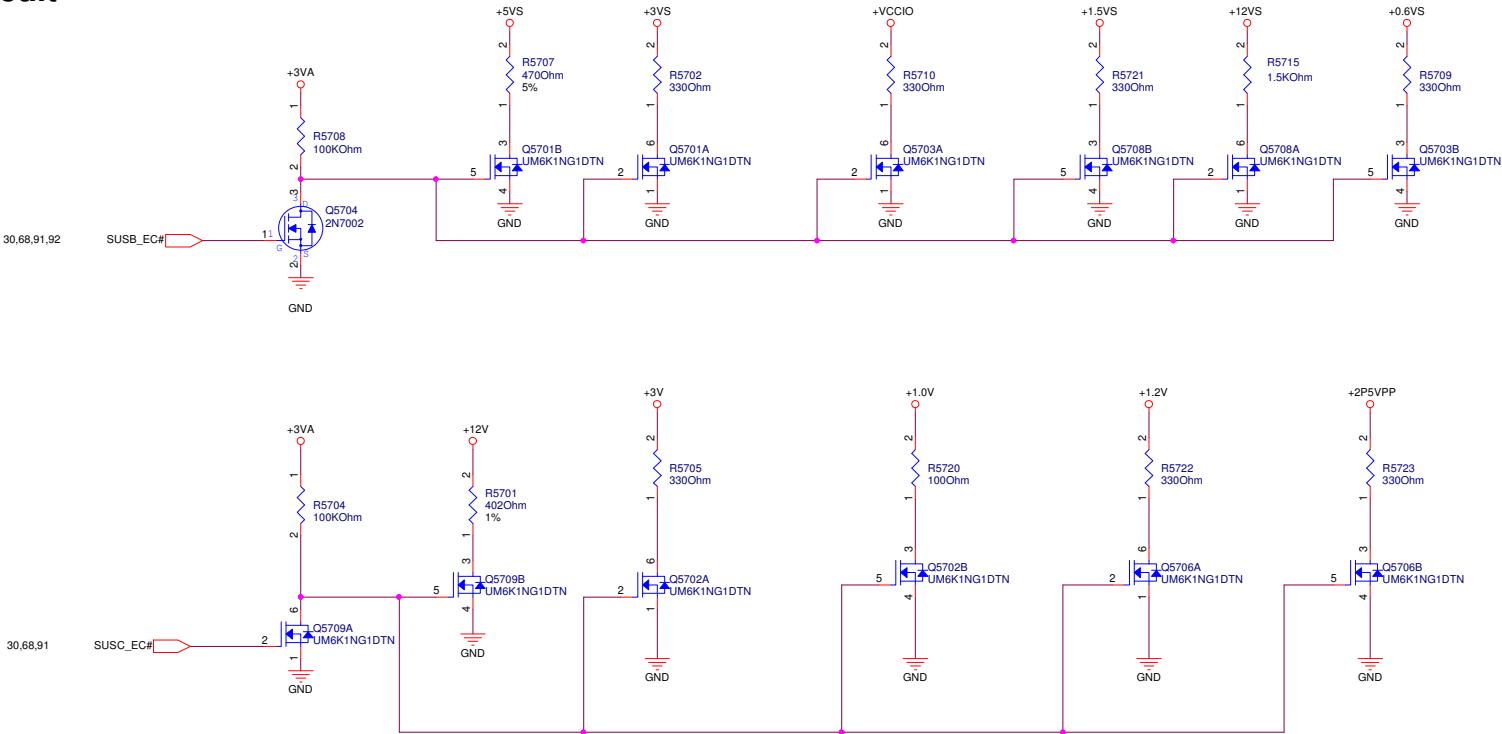


<Variant Name>

<b>PEGATRON</b>		Title : <b>LED_Indicator</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		Engineer: <b>Andy Kao</b>	
Size <b>B</b>	Project Name <b>X3</b>		Rev <b>1.0</b>
Date: <b>Wednesday, August 31, 2016</b>		Sheet	<b>56</b> of <b>97</b>



Discharge Circuit



D

C

B

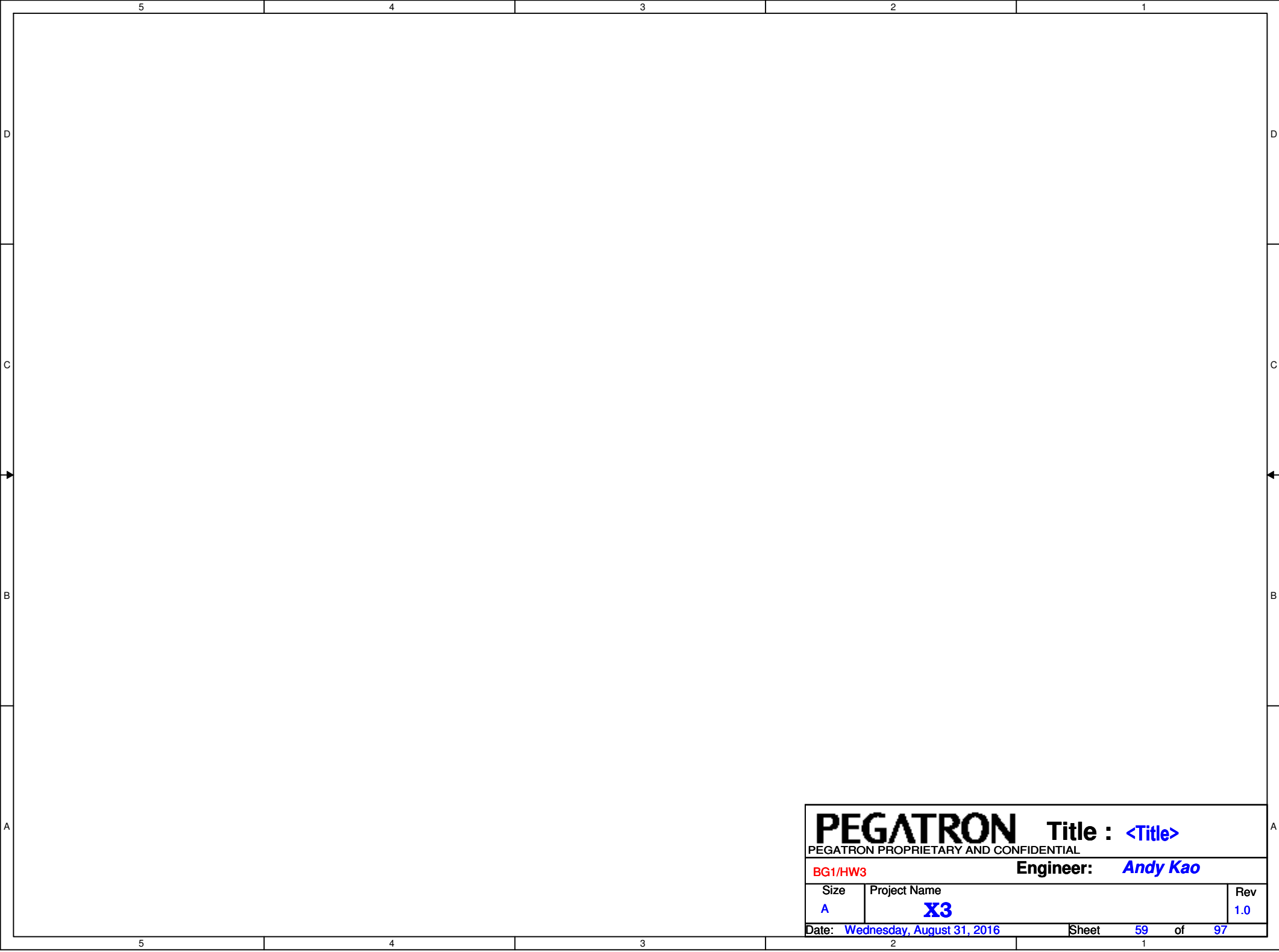
A

**PEGATRON**      Title : <Title>

**BG1/HW3** **Engineer:** *Andy Kao*

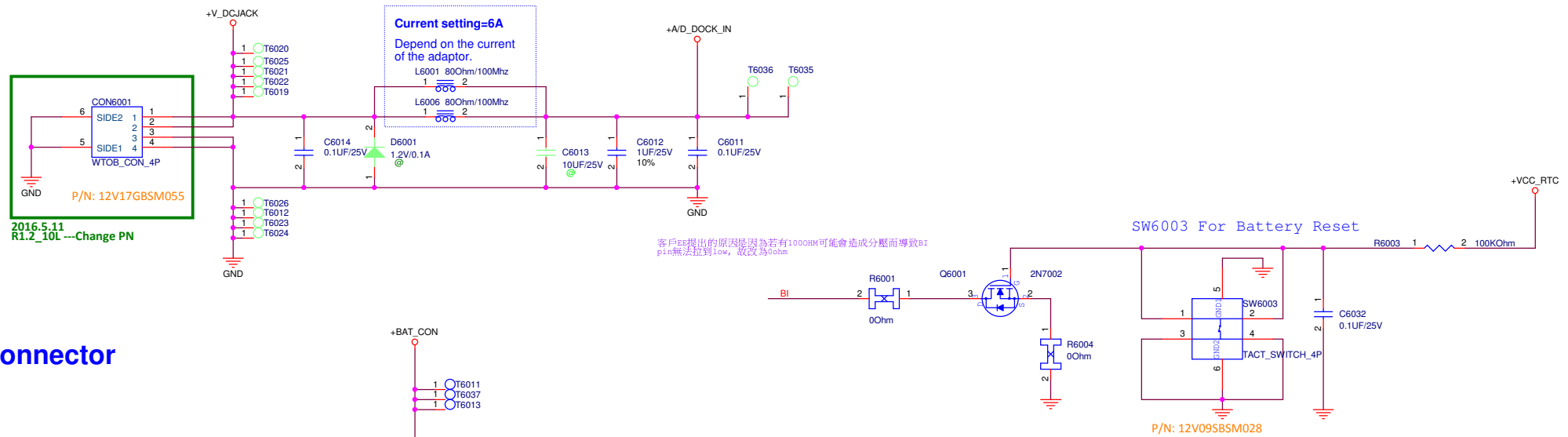
Size	Project Name	Rev
A	X3	1.0

Date: Wednesday, August 31, 2016 Sheet 58 of 97

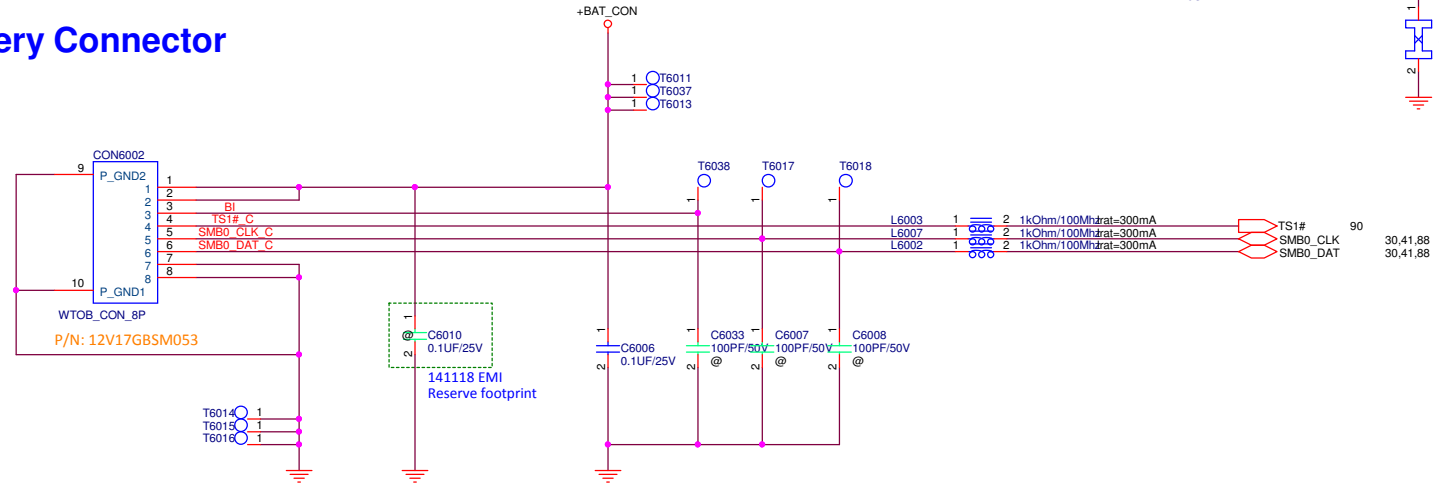


<b>PEGATRON</b> <b>Title :</b> <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>
Size <i>A</i>	Project Name <b>X3</b>	Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>59</i> of <i>97</i>

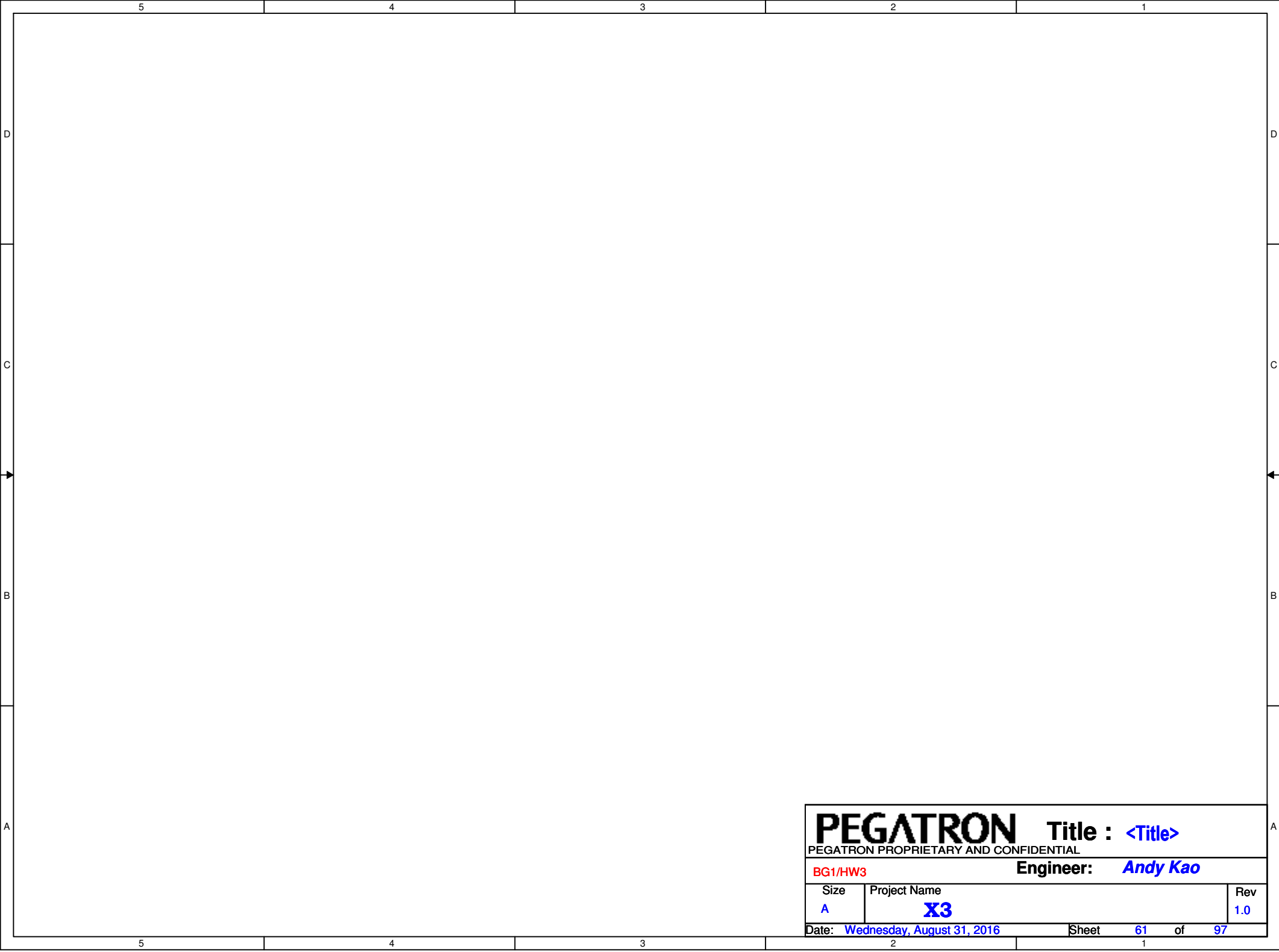
DC Jack WtoB CONN



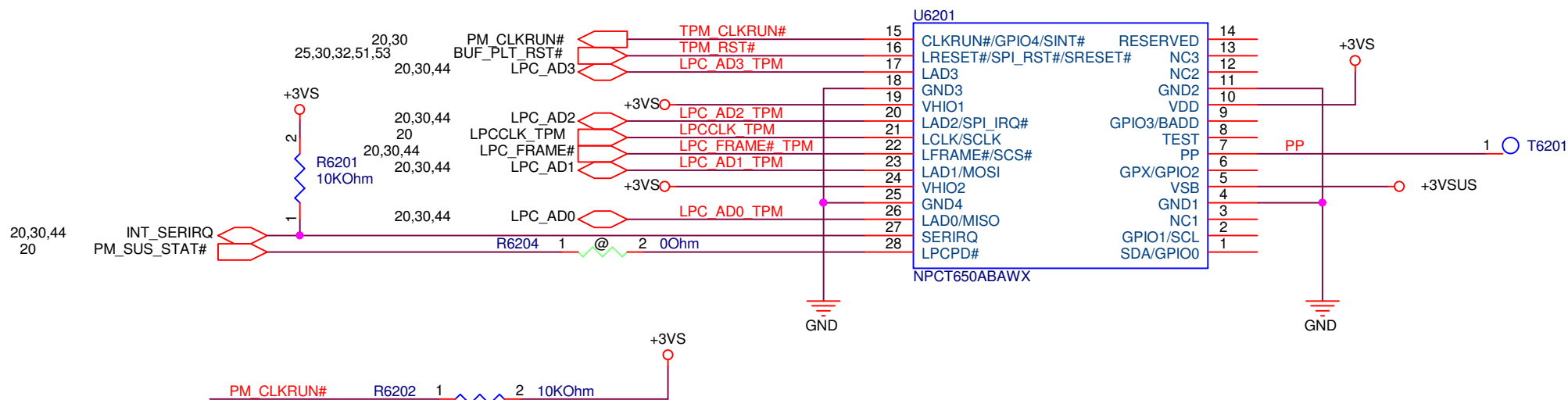
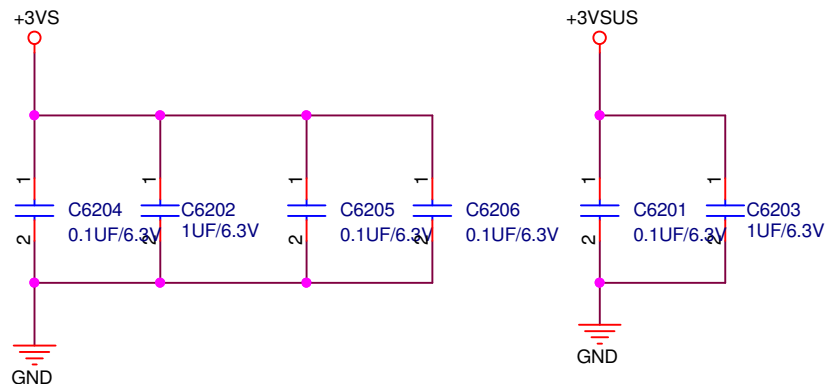
Battery Connector



PEGATRON				Title : DC_IN/BAT CONN	
BG1/HW3		Engineer: Andy Kao			
Size	Project Name			Rev	
Custom	X3			1.0	
Date: Wednesday, August 31, 2016		Sheet 60 of 97			



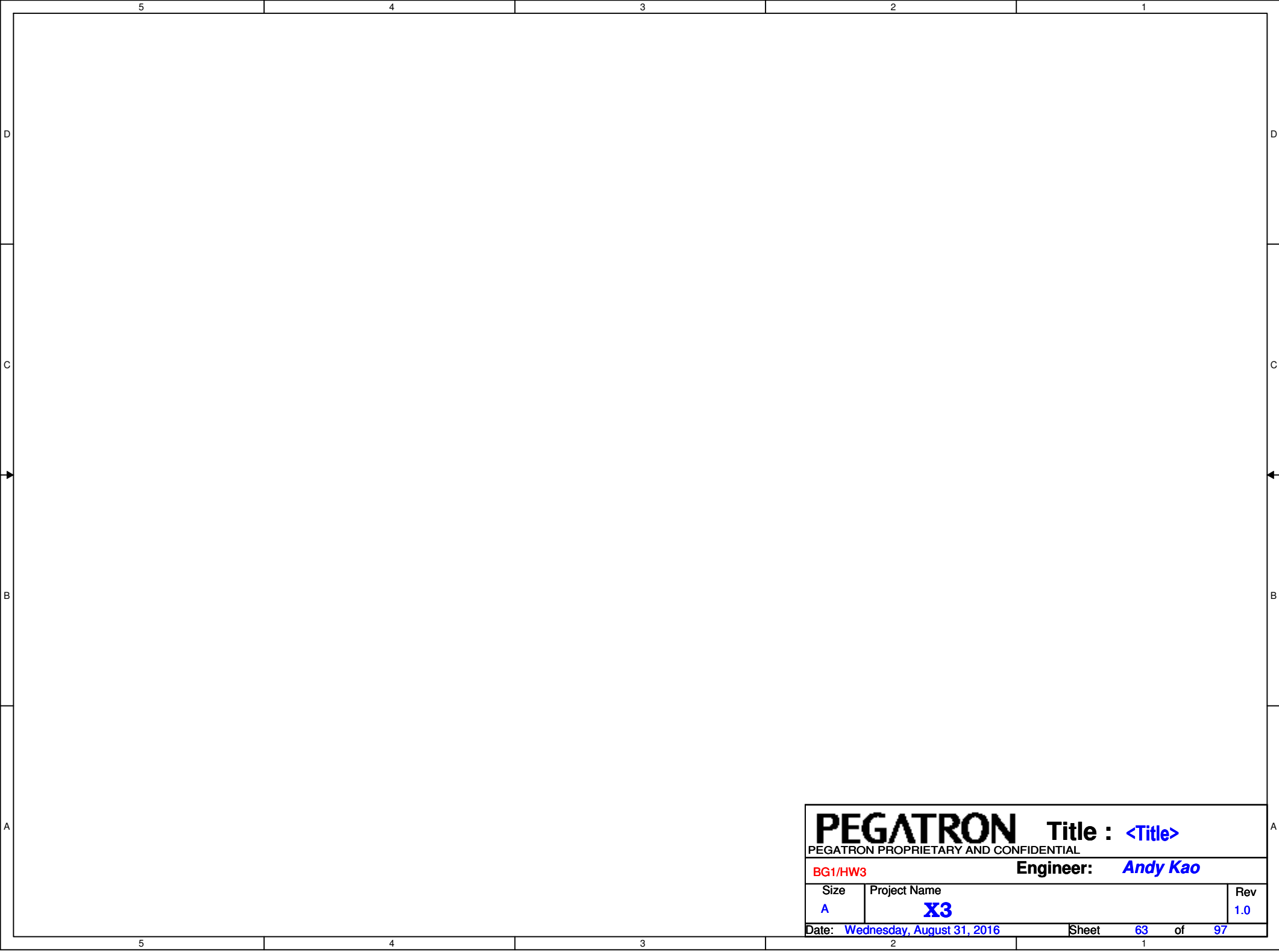
<b>PEGATRON</b> <b>Title :</b> <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>
Size <i>A</i>	Project Name <b>X3</b>	Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>61</i> of <i>97</i>



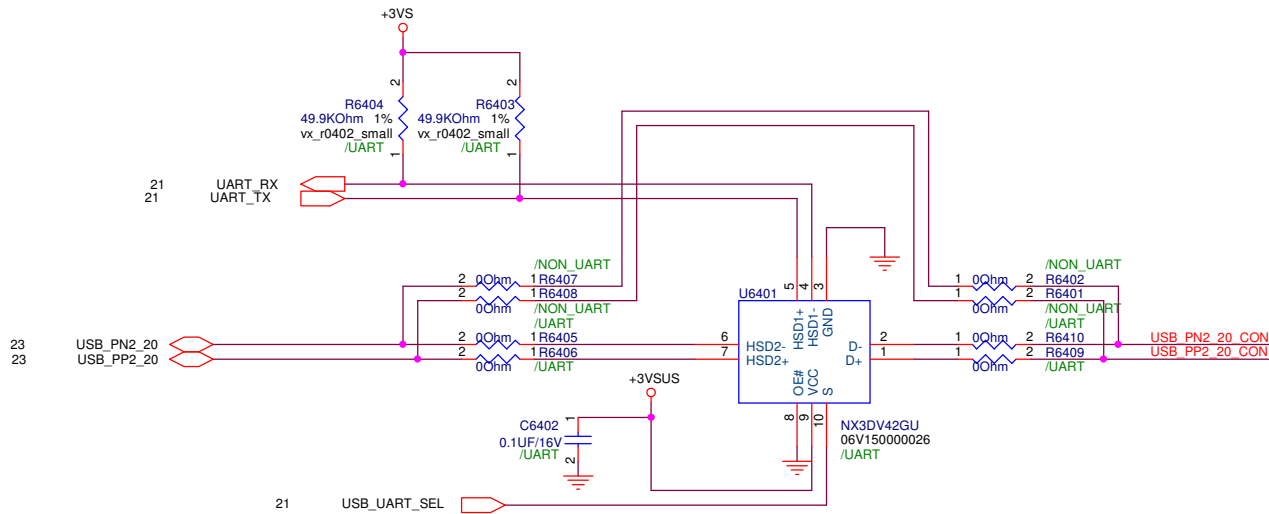
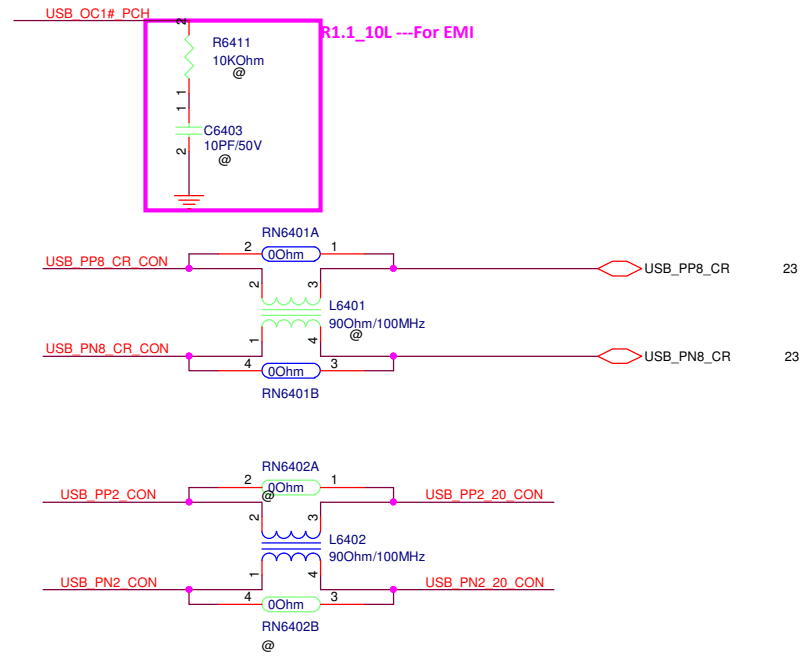
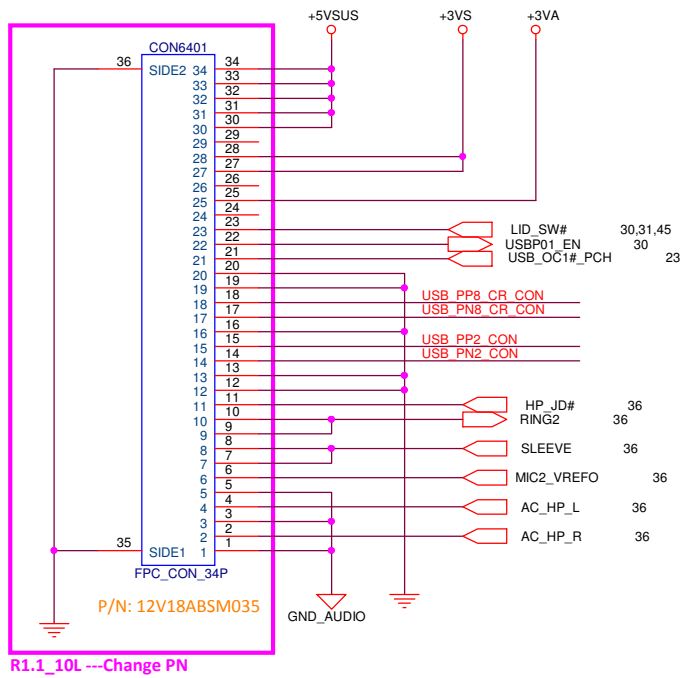
Vendor Suggest Pull High Resistor Need To Close To TPM  
PM\_CLKRUN#, INT\_SERIRQ Need To Pull 10Kohm To+3VS at Chipset Side

<Variant Name>

<b>PEGATRON</b>		Title : <b>TPM CONN</b>	
BG1/HW3		Engineer: <b>Andy Kao</b>	
Size Custom	Project Name <b>X3</b>		Rev 1.0
Date: <b>Wednesday, August 31, 2016</b>		Sheet <b>62</b> of <b>97</b>	



<b>PEGATRON</b>		<b>Title :</b> <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>	
Size <i>A</i>	Project Name <b>X3</b>		Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet	<i>63</i> of <i>97</i>



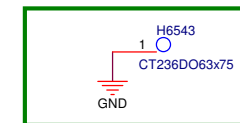
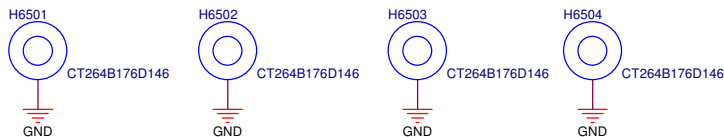
<Variant Name>		
<b>PEGATRON</b> Title : <b>IO CON.</b>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <b>Andy Kao</b>
Size B	Project Name <b>X3</b>	Rev 1.0
Date: Wednesday, August 31, 2016		Sheet 64 of 97



# CPU NUT

6\*2.5mm\*1

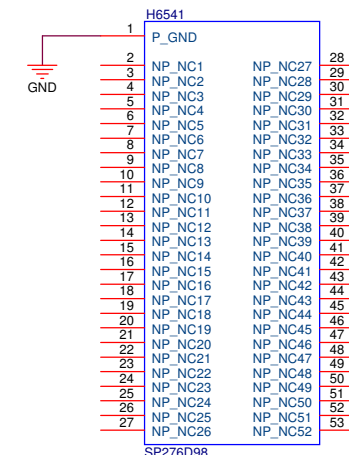
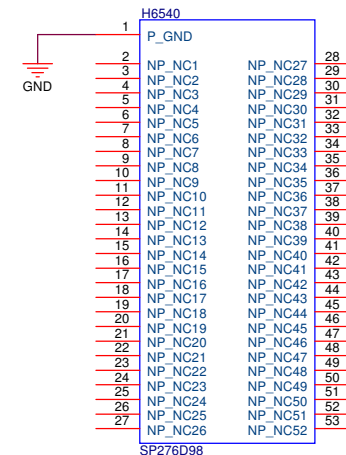
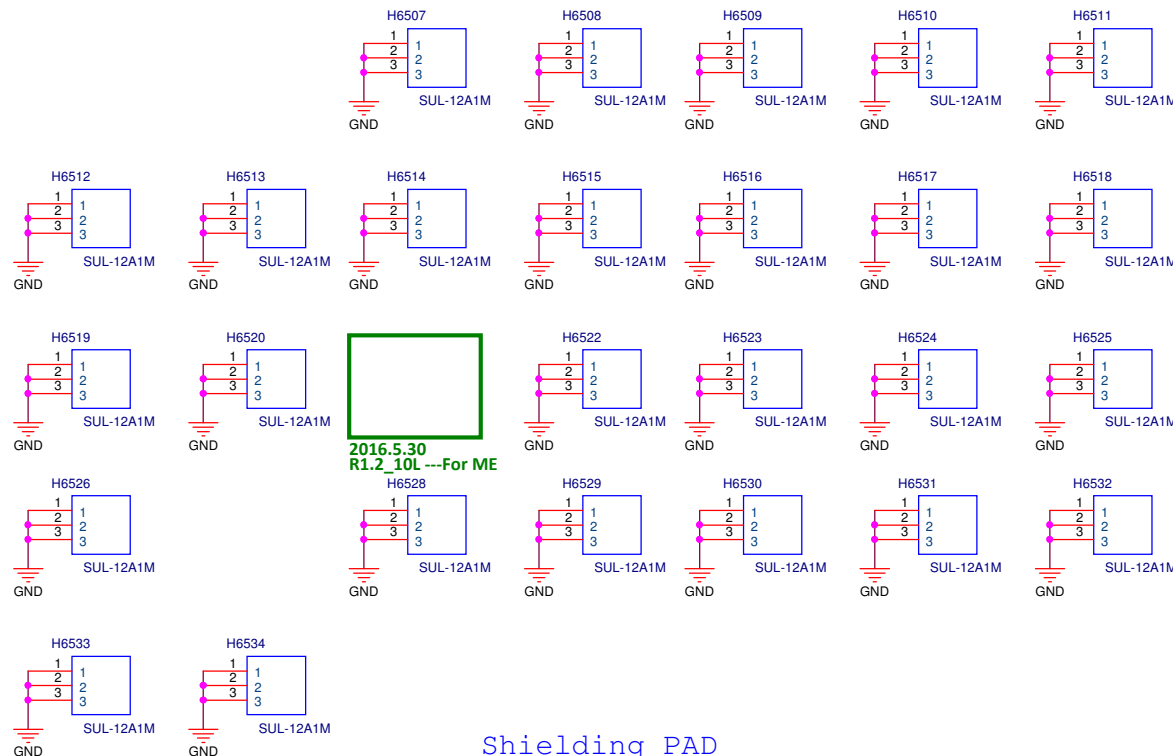
6\*3.1mm\*1



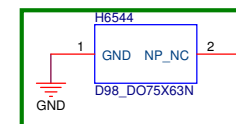
2016.6.6 R1.2\_10L ---For ME

# CLIP

Thermal screw\*2

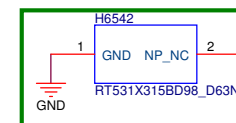


14\*8mm\*1



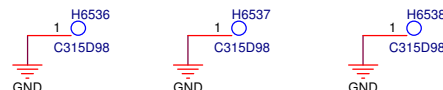
2016.6.6 R1.2\_10L ---For ME

13.5\*8mm\*1



2016.6.6 R1.2\_10L ---For ME

Shielding PAD

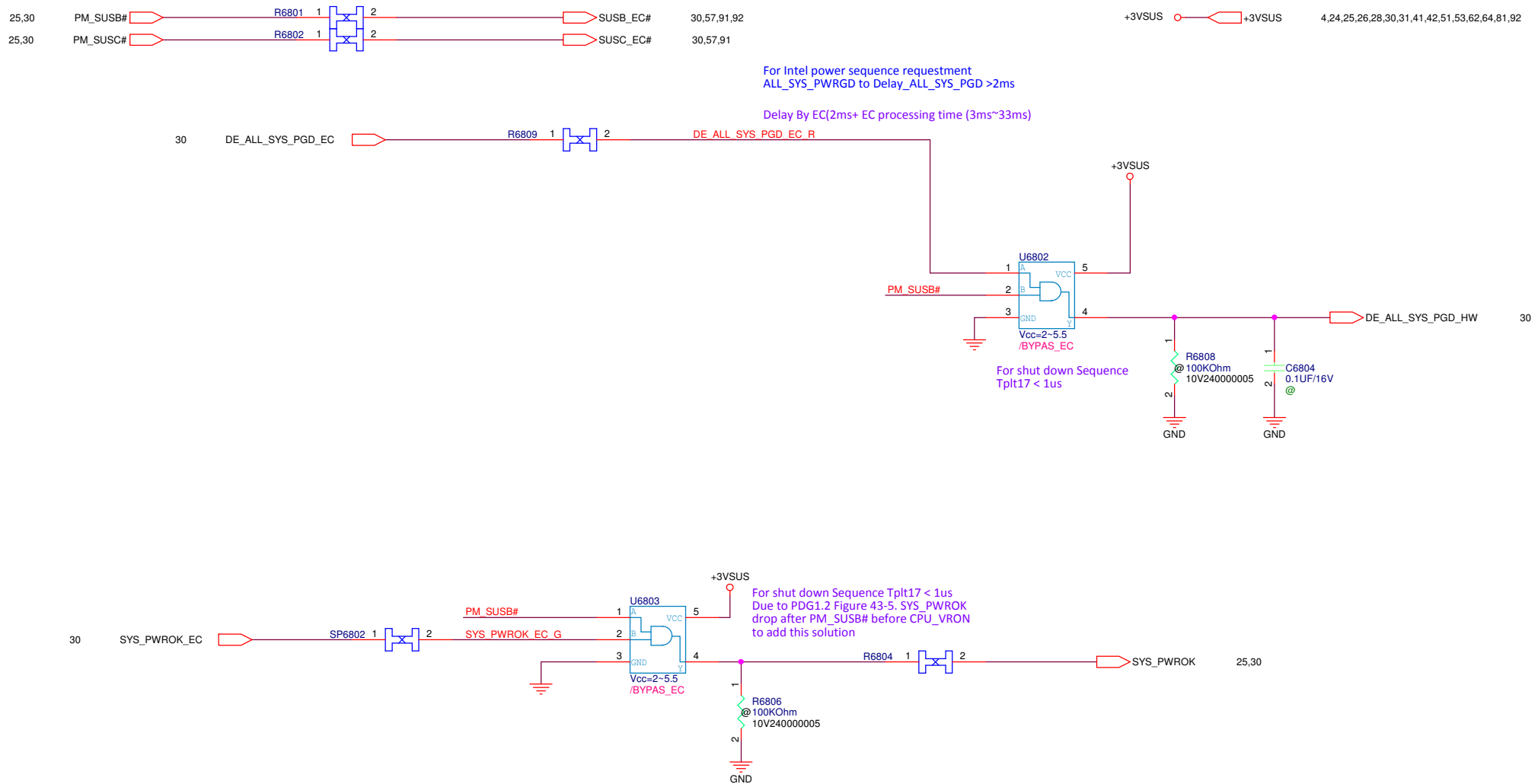


<b>PEGATRON</b>		Title : NUT,Screw Hole	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Andy Kao	
Size B	Project Name <b>X3</b>		Rev 1.0
Date: Wednesday, August 31, 2016		Sheet 65 of 97	

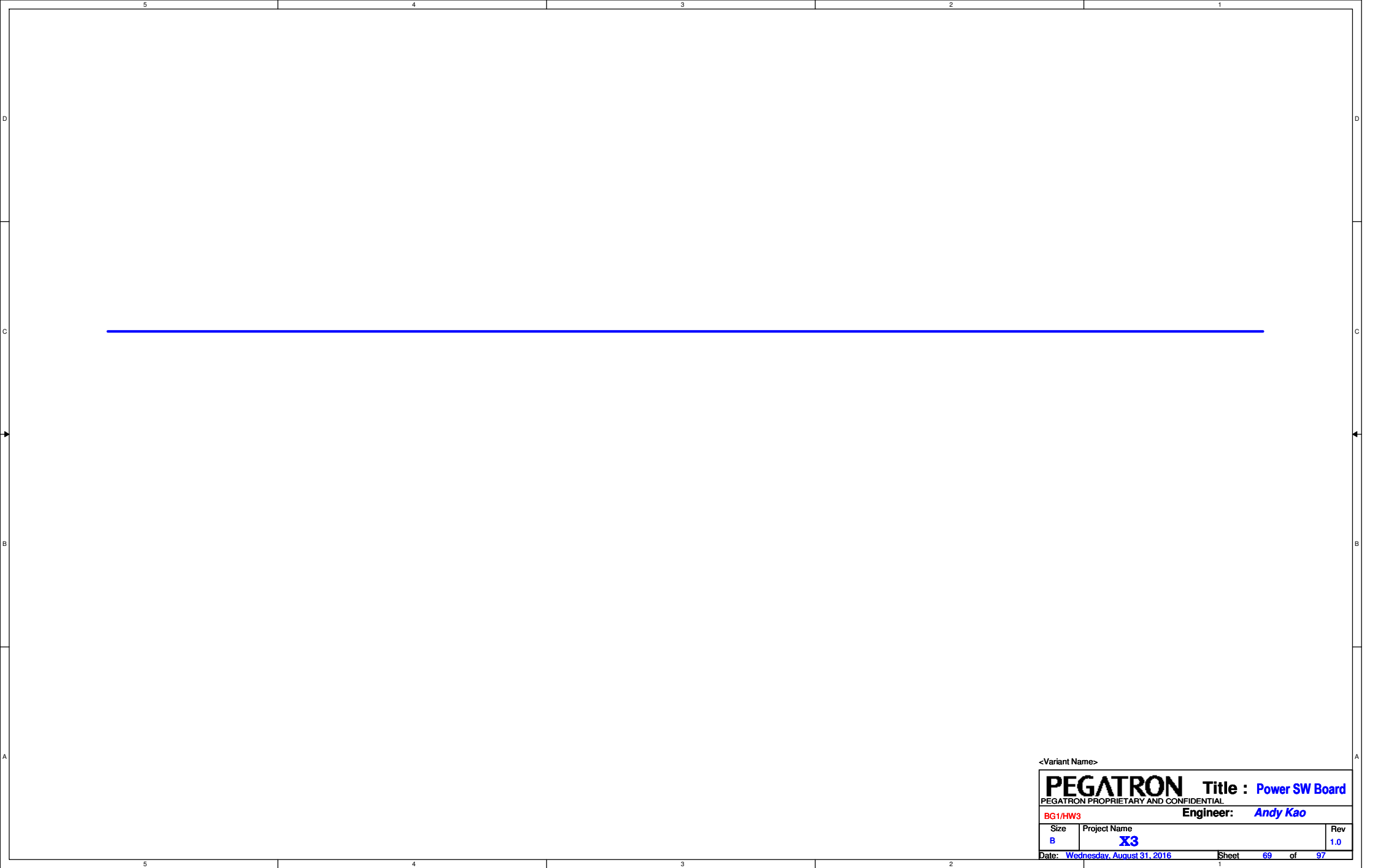
	5	4	3	2	1
D					D
C					C
B					B
A					A

<div> <div>PEGATRON</div> <div>PEGATRON PROPRIETARY AND CONFIDENTIAL</div> </div>			<div> <div>Title : &lt;Title&gt;</div> </div>		
<div> <div>BG1/HW3</div> </div>			<div> <div>Engineer:</div> <div>Andy Kao</div> </div>		
<div> <div>Size</div> <div>A</div> </div>	<div> <div>Project Name</div> <div>X3</div> </div>				<div> <div>Rev</div> <div>1.0</div> </div>
<div> <div>Date:</div> <div>Wednesday, August 31, 2016</div> </div>			<div> <div>Sheet</div> <div>66</div> </div>	<div> <div>of</div> <div>97</div> </div>	





<b>PEGATRON</b>		Title : <b>POWER Sequence</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		Engineer: <b>Andy Kao</b>	
Size <b>B</b>	Project Name <b>X3</b>		Rev <b>1.0</b>
Date: <b>Wednesday, August 31, 2016</b>		Sheet <b>68</b>	of <b>97</b>



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Size

B

Project Name

X3

Rev

1.0

Title :

Power SW Board

Engineer:

Andy Kao

Date:

Wednesday, August 31, 2016

Sheet

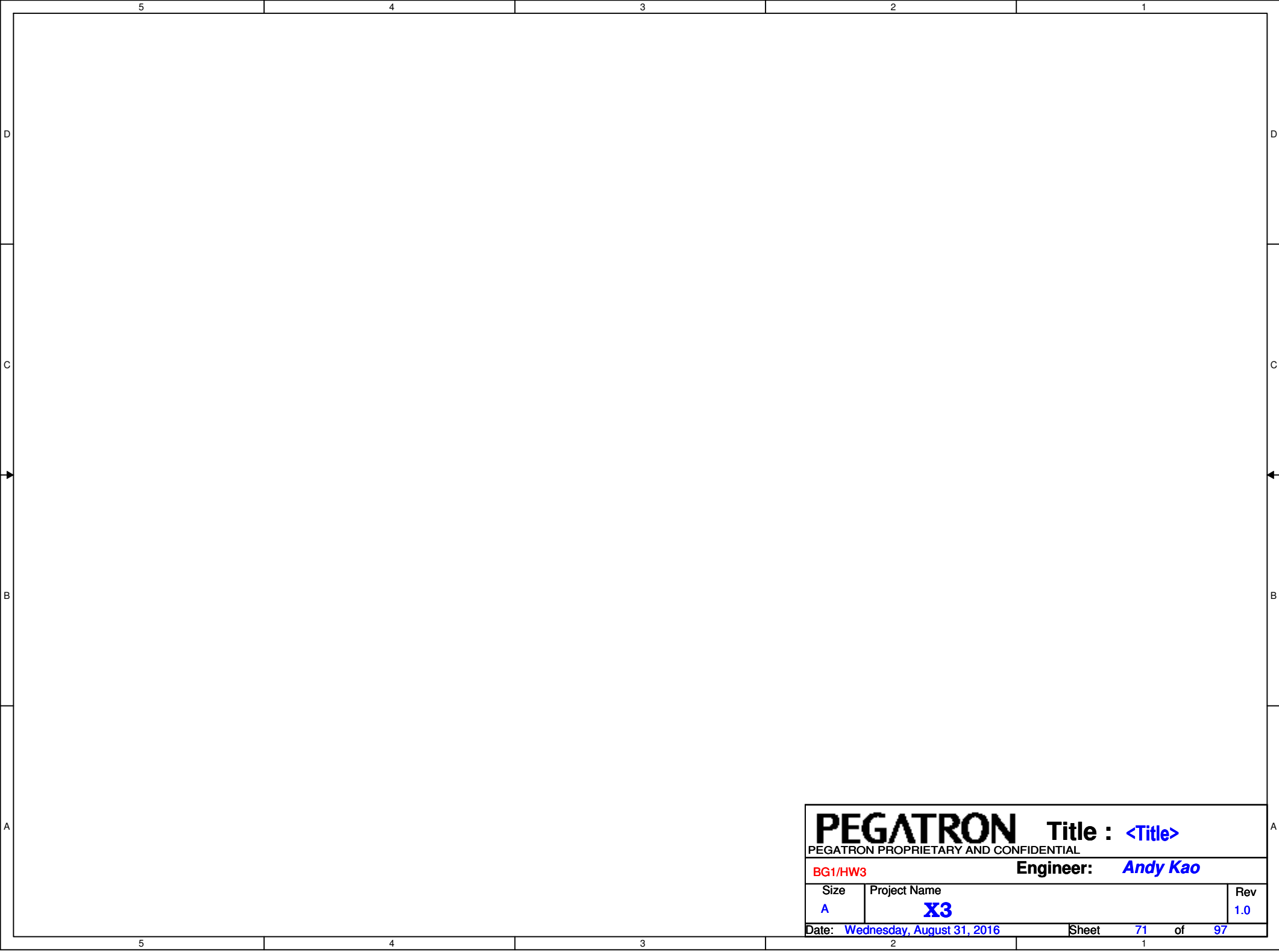
69

of

97

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D					D
C					C
B					B
A					A

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<div> <div>BG1/HW3</div> </div>			<div> <div>Engineer:</div> <div>Andy Kao</div> </div>		
<div> <div>Size</div> <div>A</div> </div>	<div> <div>Project Name</div> <div>X3</div> </div>				<div> <div>Rev</div> <div>1.0</div> </div>
<div> <div>Date:</div> <div>Wednesday, August 31, 2016</div> </div>			<div> <div>Sheet</div> <div>70</div> </div>	<div> <div>of</div> <div>97</div> </div>	

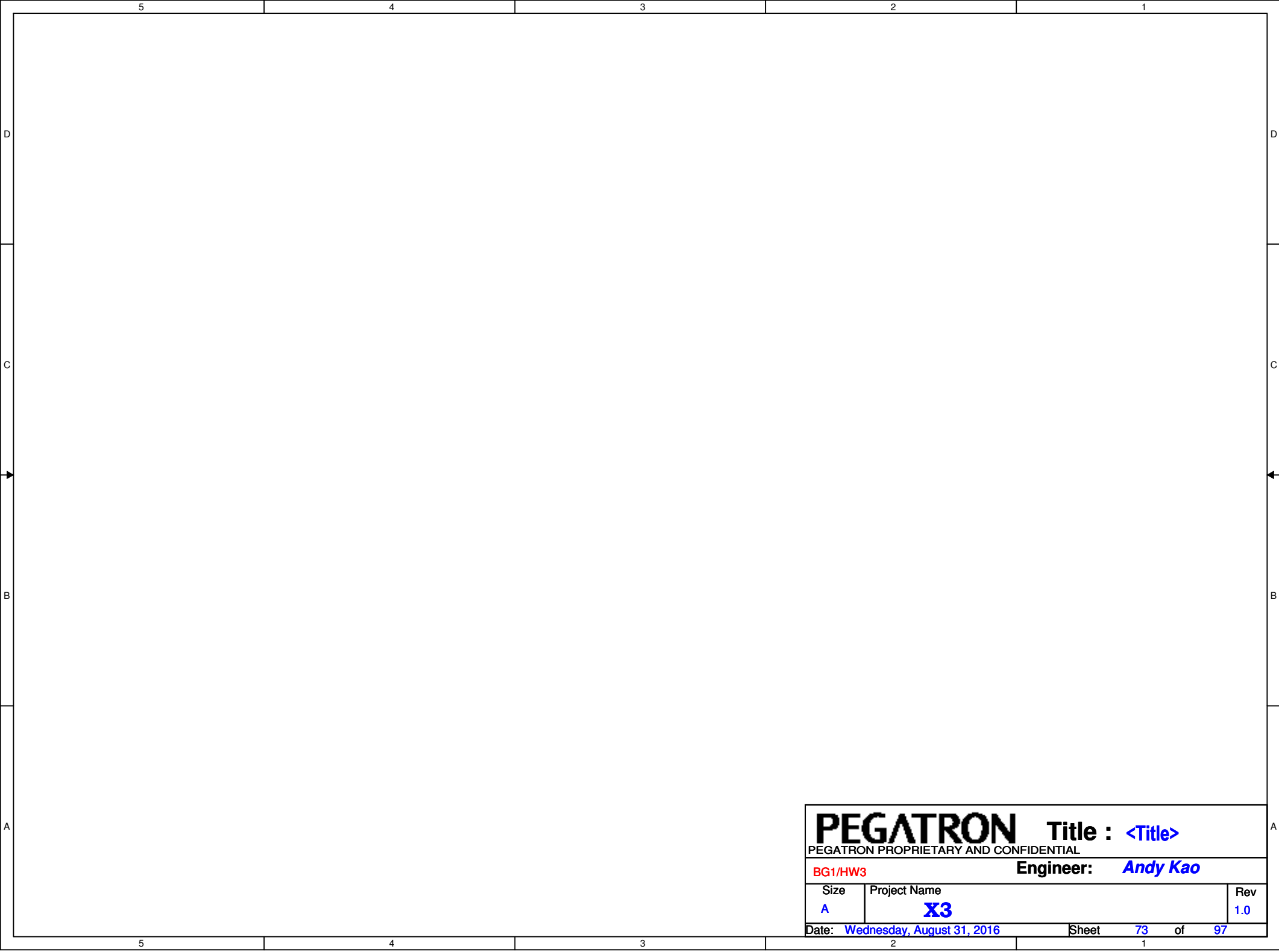


<b>PEGATRON</b> <b>Title :</b> <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>
Size <i>A</i>	Project Name <b>X3</b>	Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>71</i> of <i>97</i>

	5	4	3	2	1
D					D
C					C
B					B
A					A

<div> <div>PEGATRON</div> <div>Title : &lt;Title&gt;</div> </div> <div>PEGATRON PROPRIETARY AND CONFIDENTIAL</div>		
<div>BG1/HW3</div>		<div>Engineer: Andy Kao</div>
<div>Size</div> <div>A</div>	<div>Project Name</div> <div>X3</div>	<div>Rev</div> <div>1.0</div>
<div>Date: Wednesday, August 31, 2016</div>		<div>Sheet 72 of 97</div>

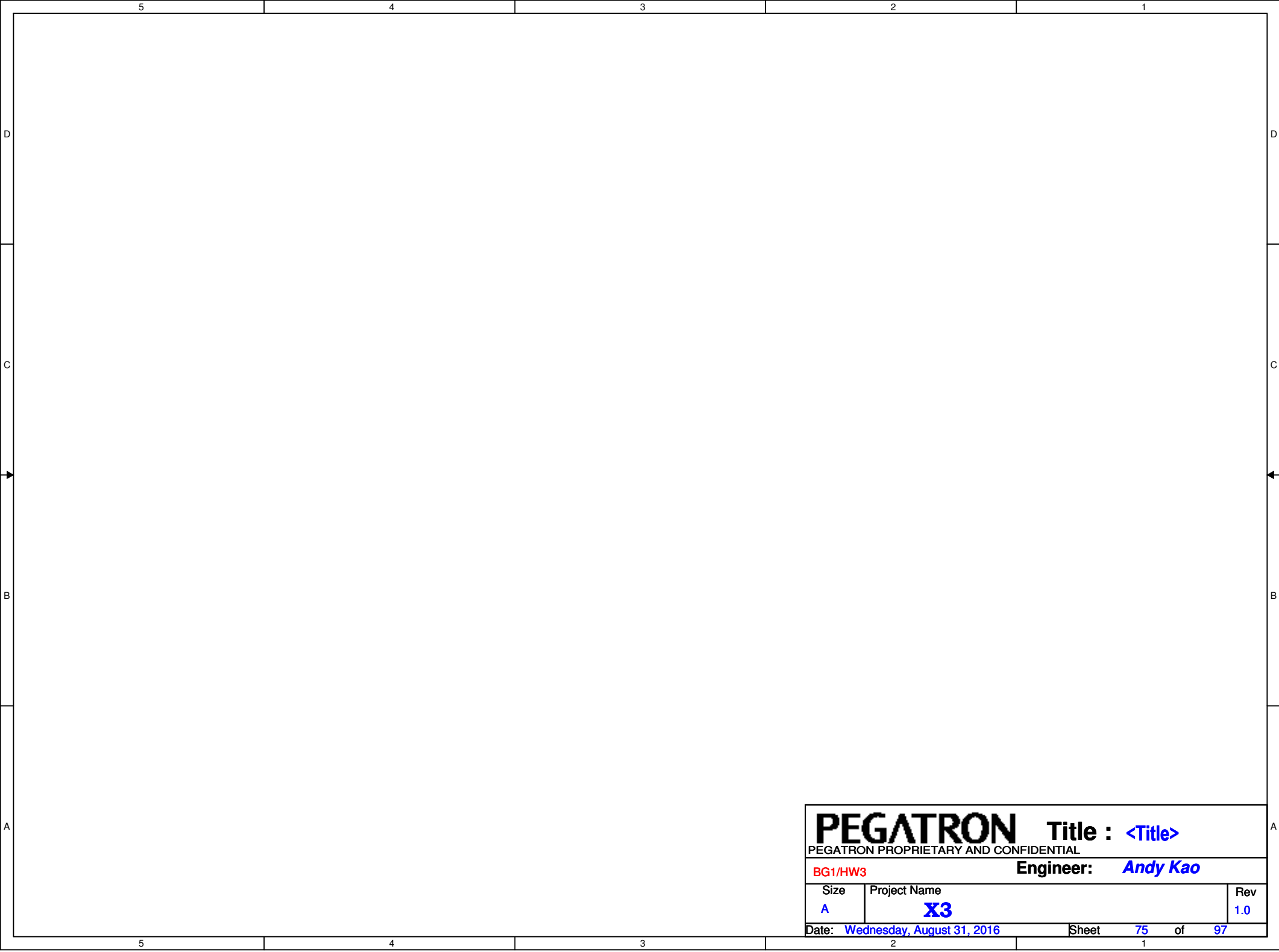




<b>PEGATRON</b> <b>Title :</b> <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>
Size <b>A</b>	Project Name <b>X3</b>	Rev <b>1.0</b>
Date: <b>Wednesday, August 31, 2016</b>		Sheet <b>73</b> of <b>97</b>

	5	4	3	2	1
D					D
C					C
B					B
A					A

<div> <div>PEGATRON</div> <div>PEGATRON PROPRIETARY AND CONFIDENTIAL</div> </div>			<div> <div>Title : &lt;Title&gt;</div> </div>		
<div> <div>BG1/HW3</div> </div>			<div> <div>Engineer:</div> <div>Andy Kao</div> </div>		
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<div> <div>Date:</div> <div>Wednesday, August 31, 2016</div> </div>			<div> <div>Sheet</div> <div>74</div> </div>	<div> <div>of</div> <div>97</div> </div>	



<b>PEGATRON</b> Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: <i>Andy Kao</i>
Size <i>A</i>	Project Name <b>X3</b>	Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>75</i> of <i>97</i>

D

C

B

A |

**PEGATRON** Title : <Title>

**PEGATRON PROPRIETARY AND CONFIDENTIAL**

BG1/HW3

**Engineer:** *Andy Kao*

Size

A

Project Name
--------------

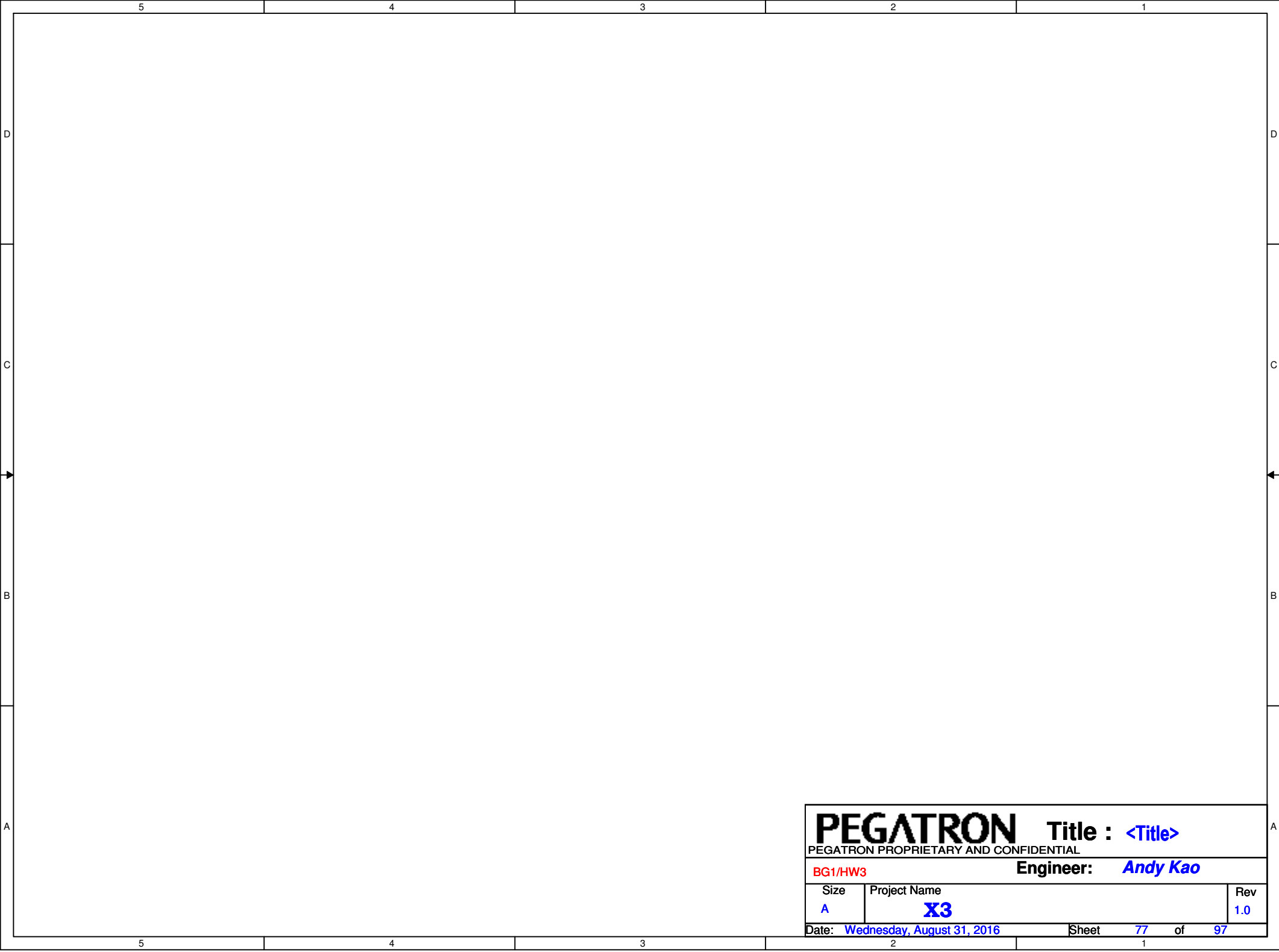
### X3

Rev

1.0

Date: Wednesday, August 31, 2016

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<b>PEGATRON</b>		<b>Title :</b> <Title>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		<b>Engineer:</b> <i>Andy Kao</i>	
Size <i>A</i>	Project Name <b>X3</b>		Rev <i>1.0</i>
Date: <i>Wednesday, August 31, 2016</i>		Sheet <i>77</i> of <i>97</i>	

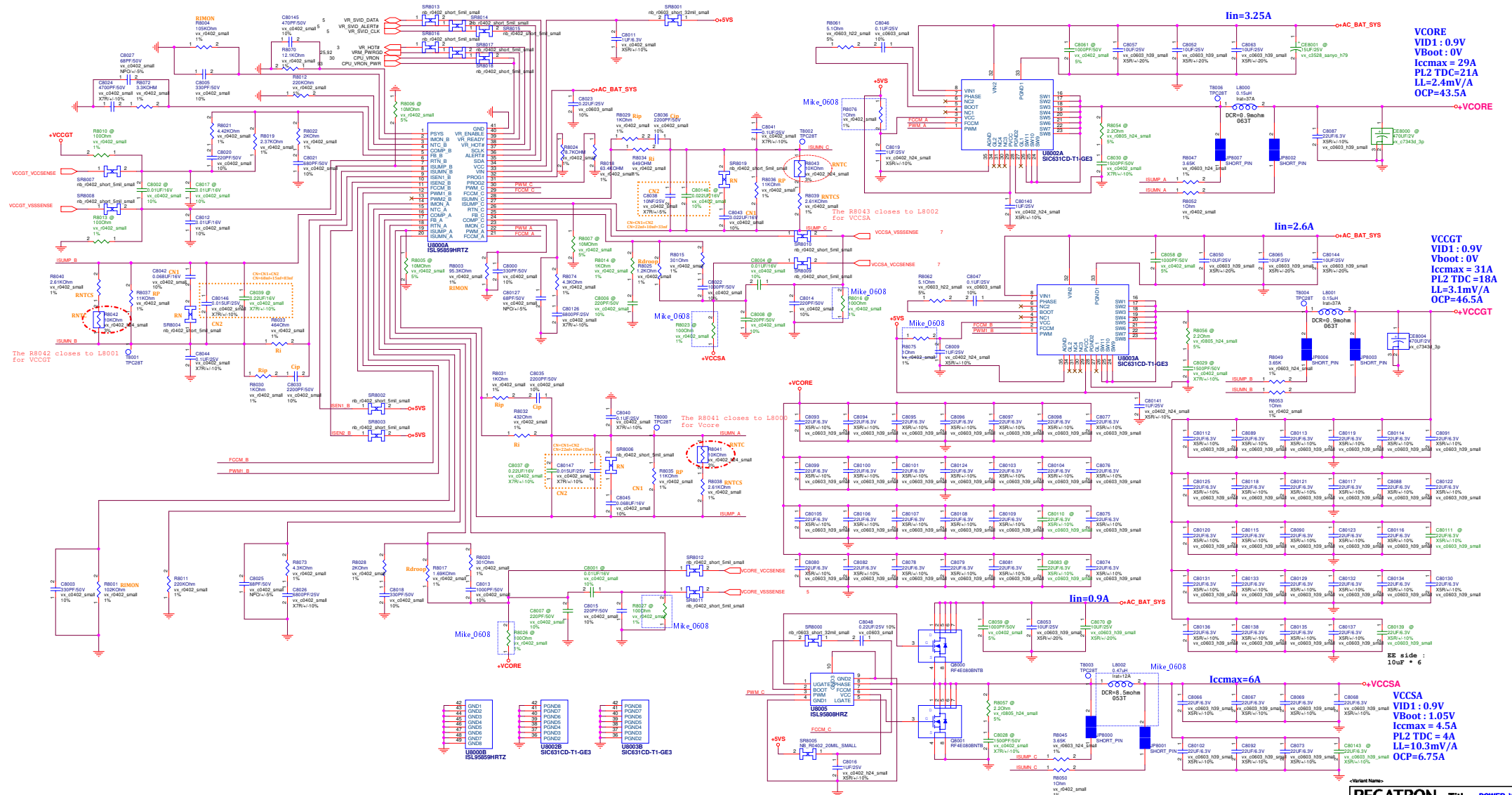


<b>PEGATRON</b> Title : <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3		Engineer: Andy Kao
Size A	Project Name X3	Rev 1.0
Date: Wednesday, August 31, 2016		Sheet 78 of 97

5					4					3					2					1									
D																													
C																													
B																													
A																													
5										4					3					2					1				

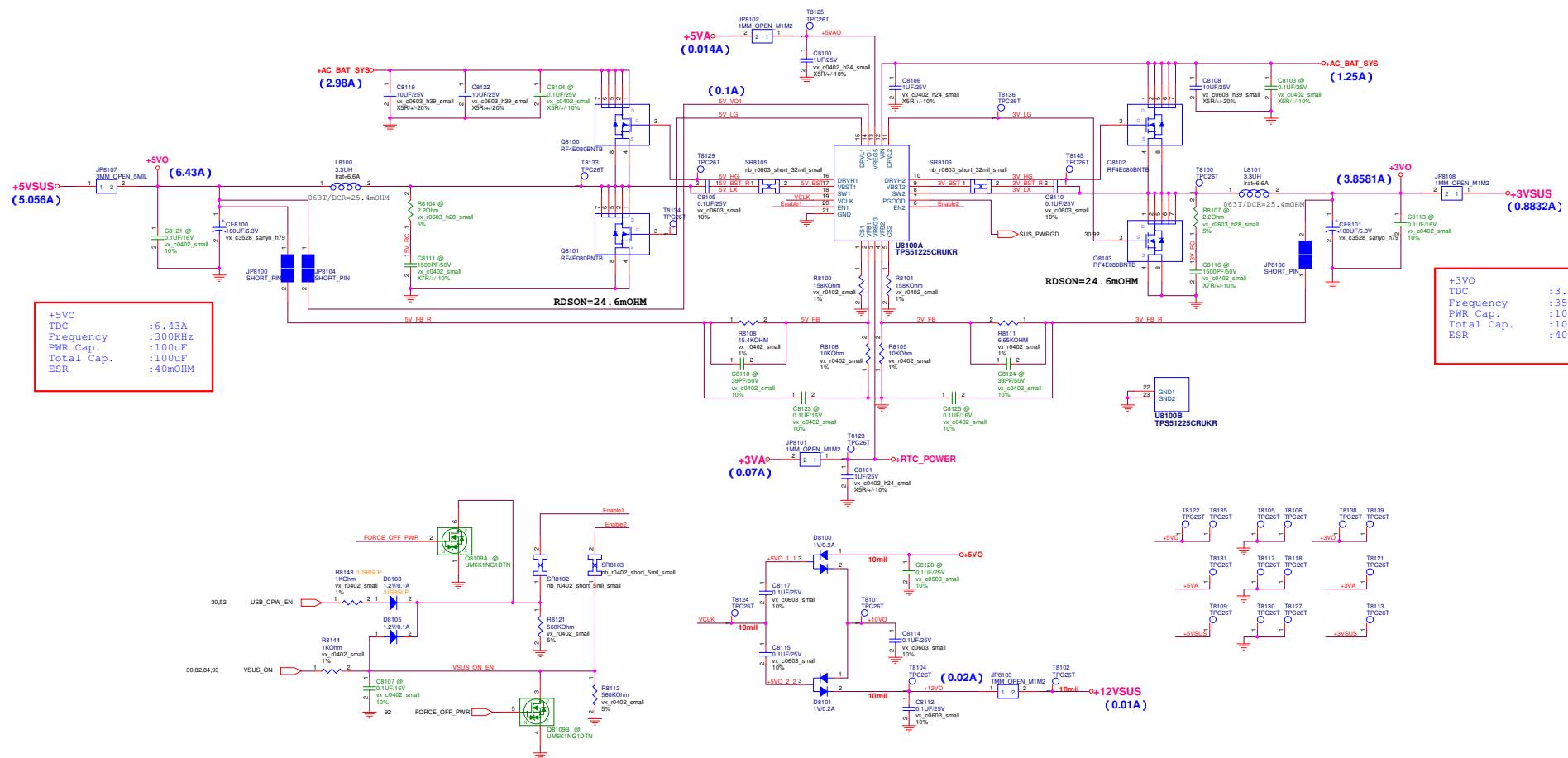
<b>PEGATRON</b>			<b>Title :</b> <Title>		
PEGATRON PROPRIETARY AND CONFIDENTIAL					
<b>BG1/HW3</b>			<b>Engineer:</b> <i>Andy Kao</i>		
Size	Project Name				Rev
A	X3				1.0
Date: <i>Wednesday, August 31, 2016</i>			Sheet <i>79</i> of <i>97</i>		

# VCORE & VCCGT & VCCSA POWER SUPPLY

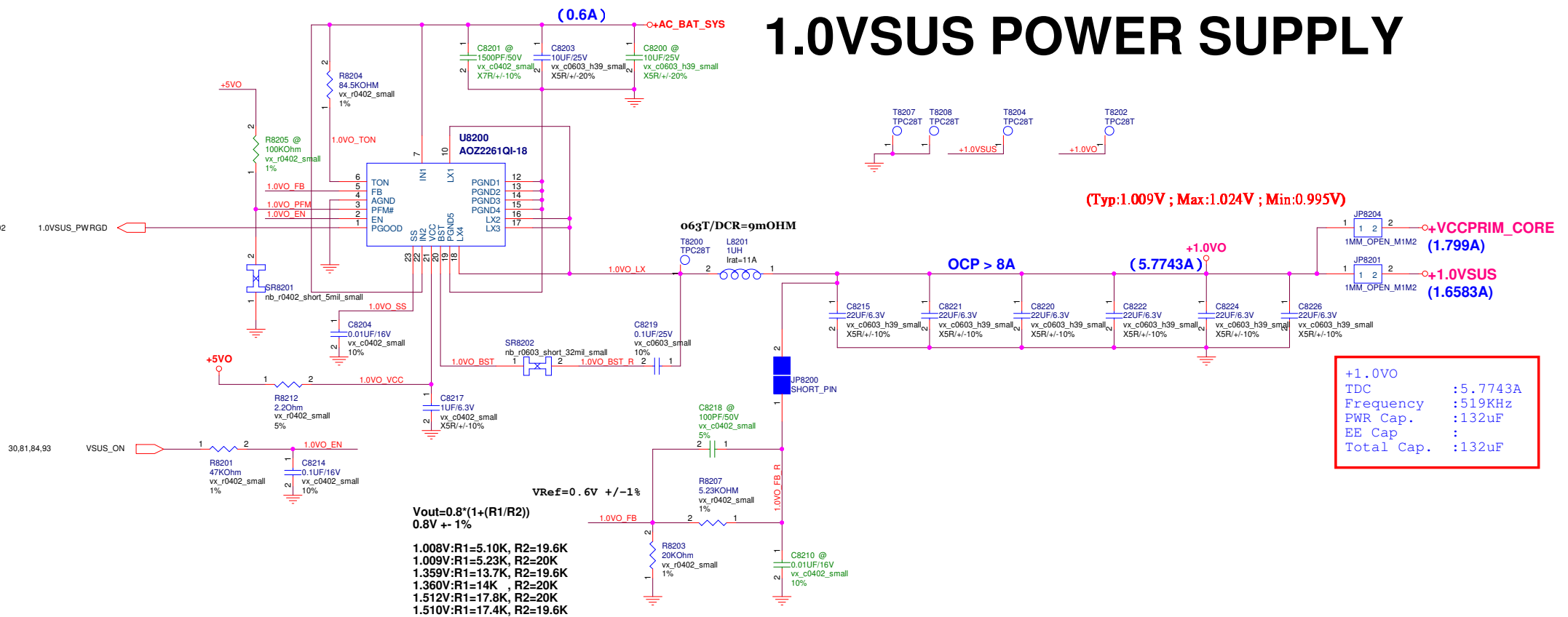




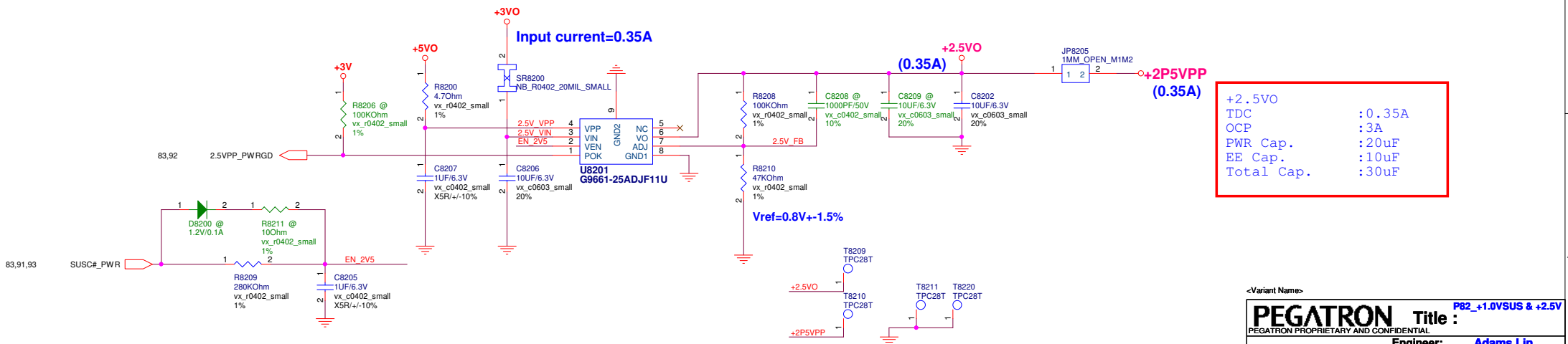
## 5VO & 3VO POWER SUPPLY



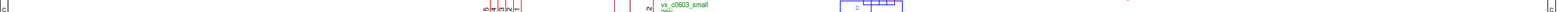
## 1.0VSUS POWER SUPPLY



## 2.5V POWER SUPPLY

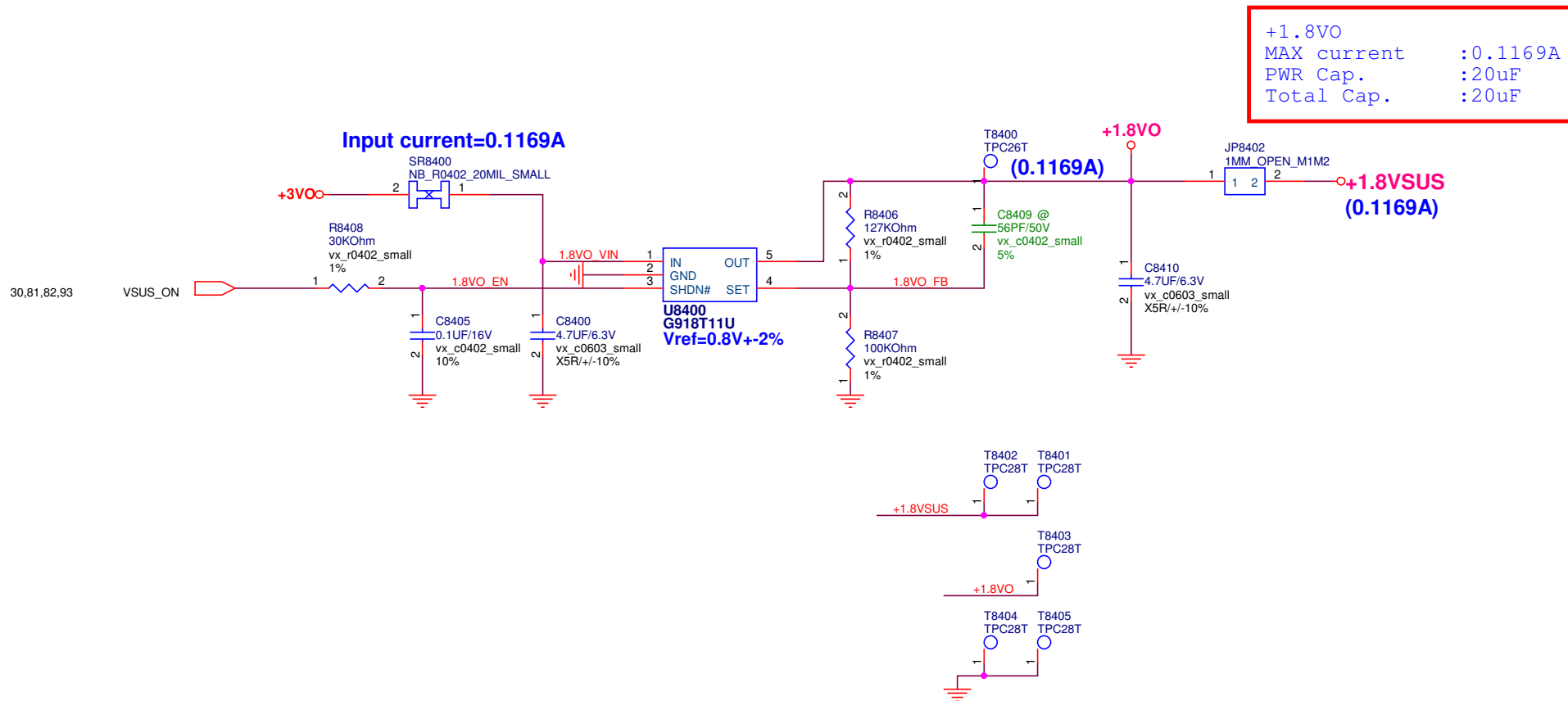


## DBIT & VHF POWER SUPPLY

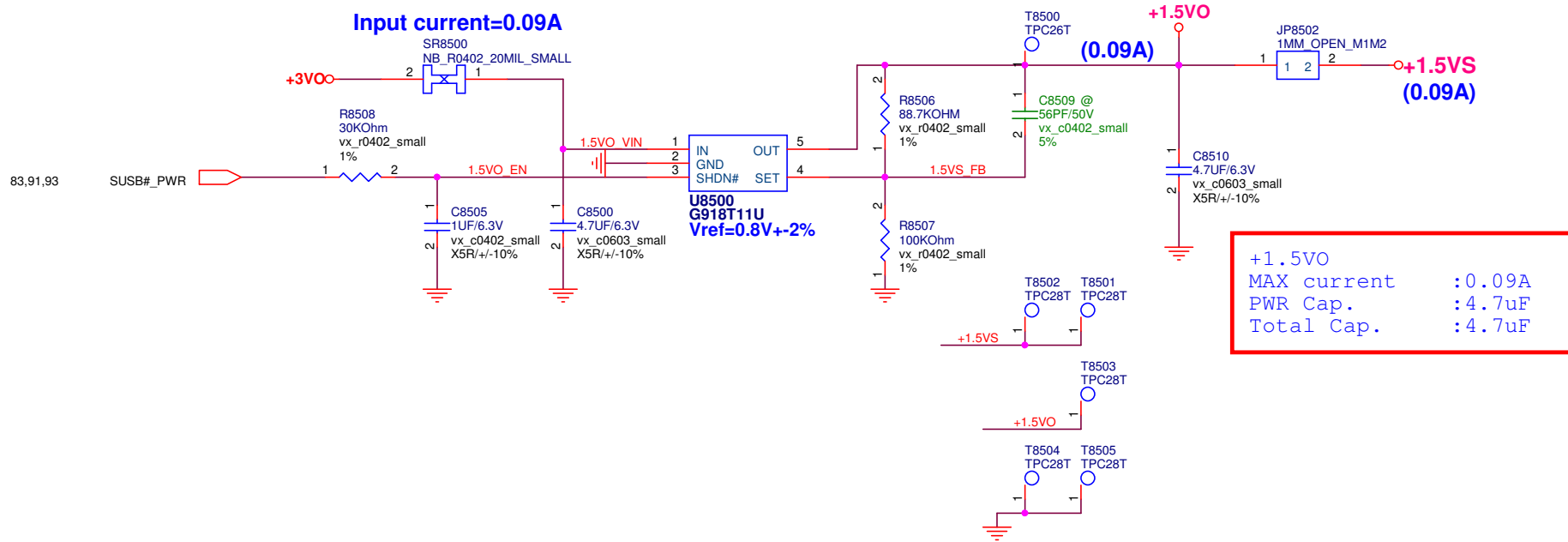
[illegible]

Date:	Wednesday, August 31, 2016	Sheet	83	of	94	1.1
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## 1.8VSUS POWER SUPPLY



## 1.5VS POWER SUPPLY



<Variant Name>

PEGATRON Title : POWER\_+1.5VS

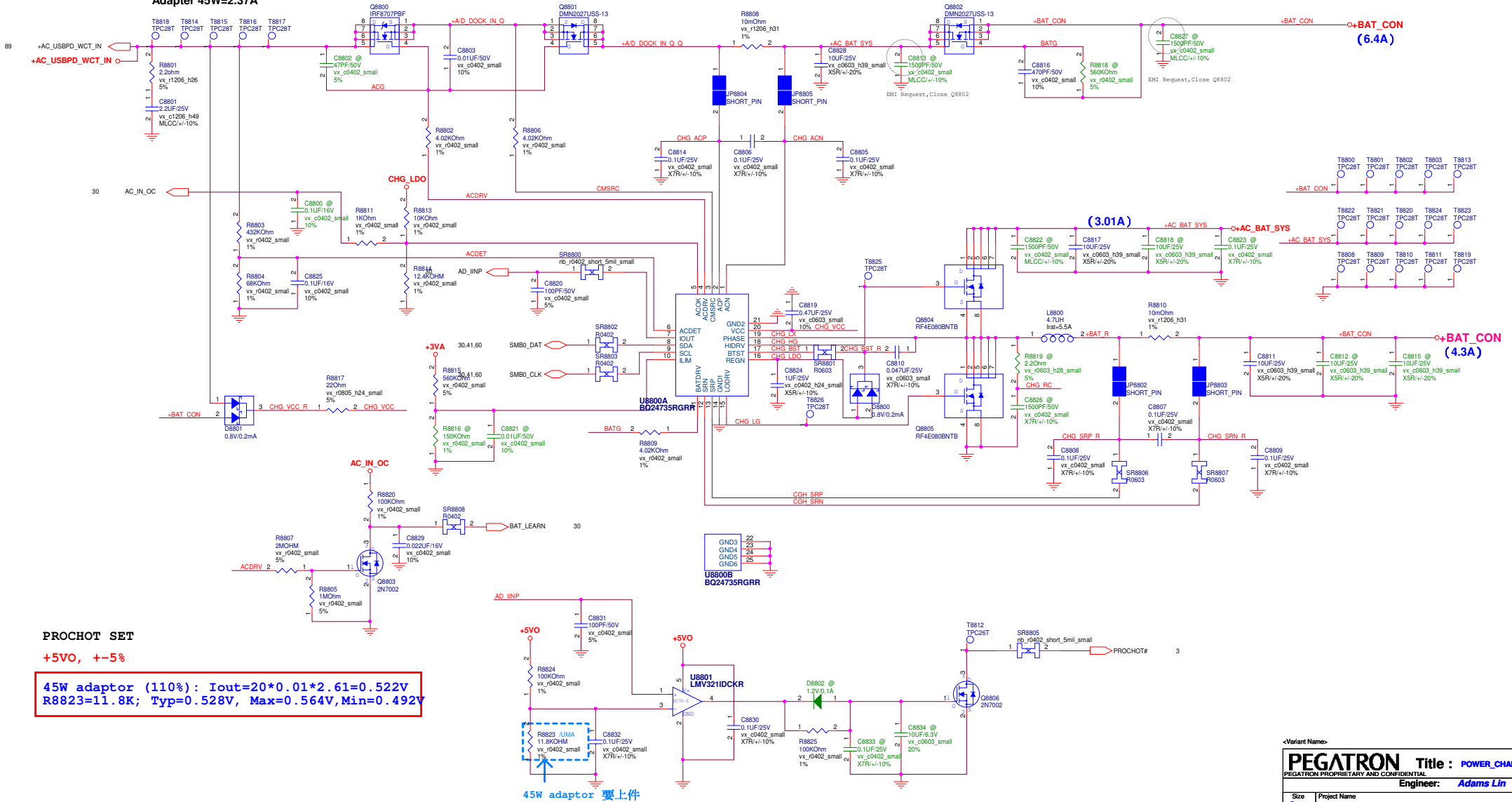
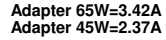
**Engineer:** Adams Lin

Size Custom	Project Name <b>X3</b>	Rev
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Date: Wednesday, August 31, 2016

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## BATTERY CHARGER



PROCHOT SET

+5V0, +−5%

45W adaptor (110%):  $I_{out}=20 \times 0.01 \times 2.61=0.522V$   
R8823=11.8K; Typ=0.528V, Max=0.564V, Min=0.492V

45W adaptor 要上件

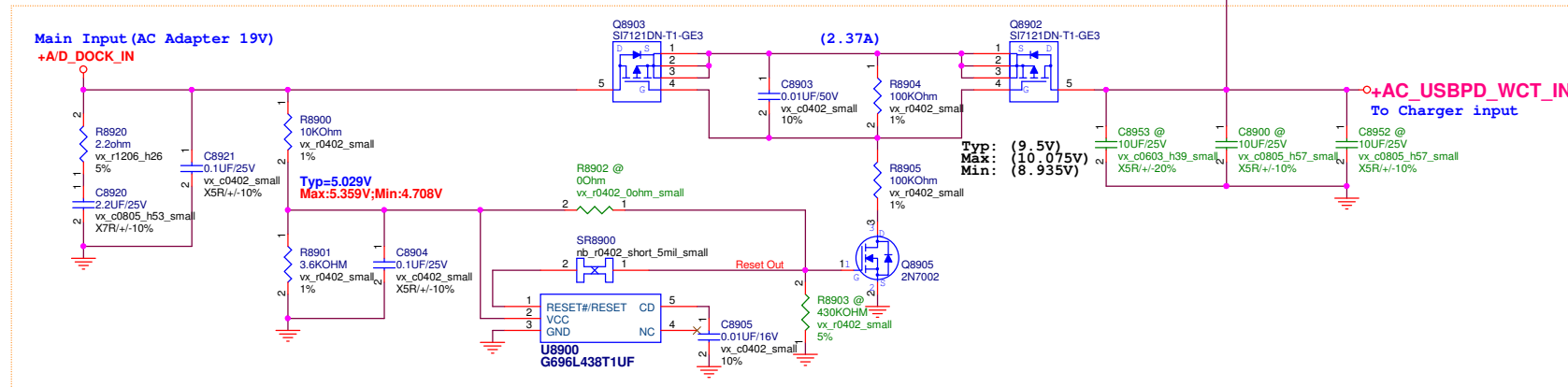
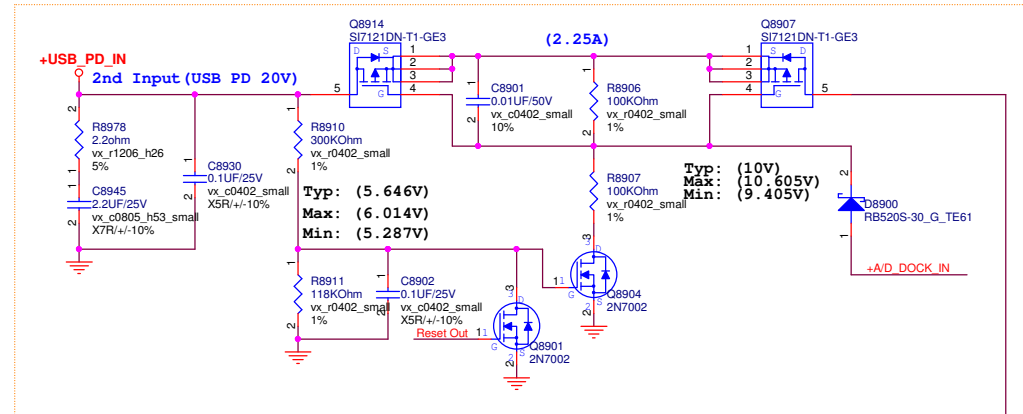
<Variant Name>

**PEGATRON** Title : **POWER\_CHARGER**  
PEGATRON PROPRIETARY AND CONFIDENTIAL

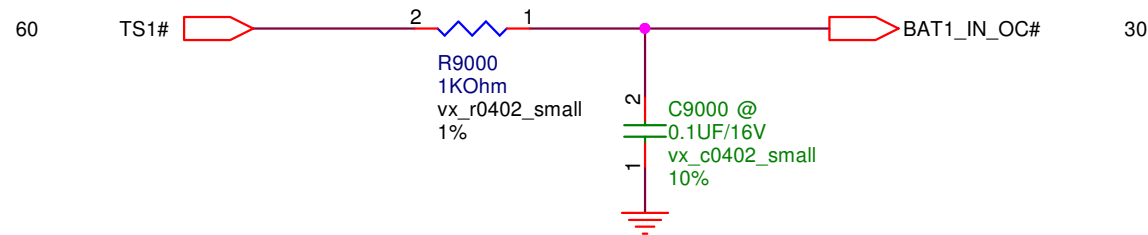
**Engineer:** *Adams Lin*

Size Custom	Project Name <b>X3</b>	Rev 1.1
Date:	Wednesday, August 31, 2016	Sheet 88 of 94

# 2 Input switch Circuit



## BATTERY IN DETECT



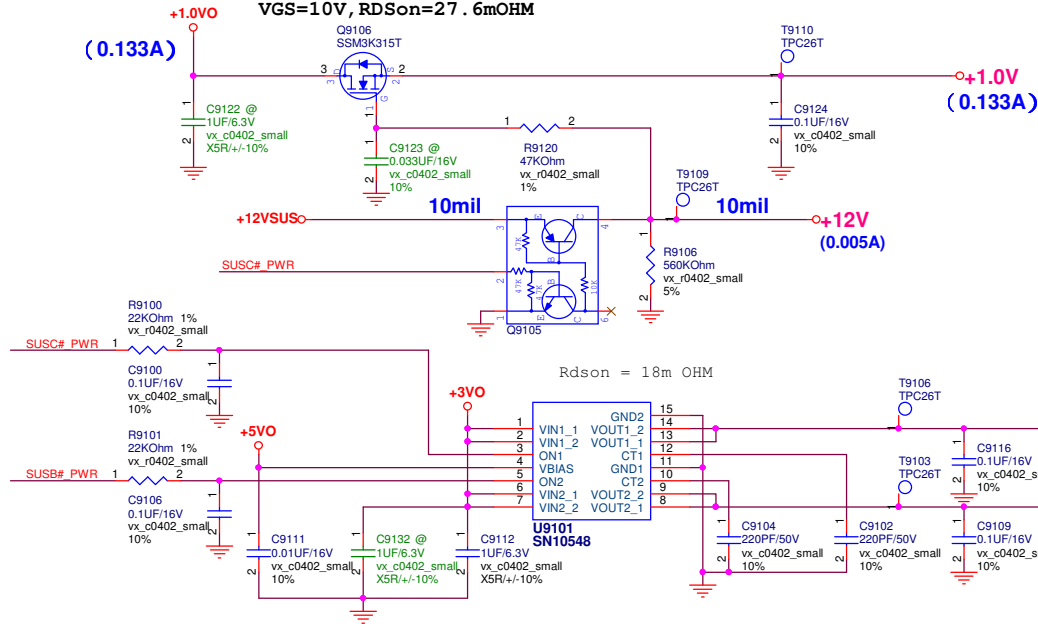
<Variant Name>

<b>PEGATRON</b>		Title : <b>POWER_DETECT</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: <b>Adams Lin</b>	
Size <b>Custom</b>	Project Name <b>X3</b>		Rev <b>1.1</b>
Date:	<b>Wednesday, August 31, 2016</b>	Sheet	<b>90</b> of <b>94</b>

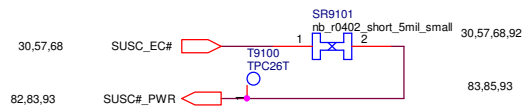


## SUSC#\_PWR POWER

VGS=10V, RDson=27.6mOHM

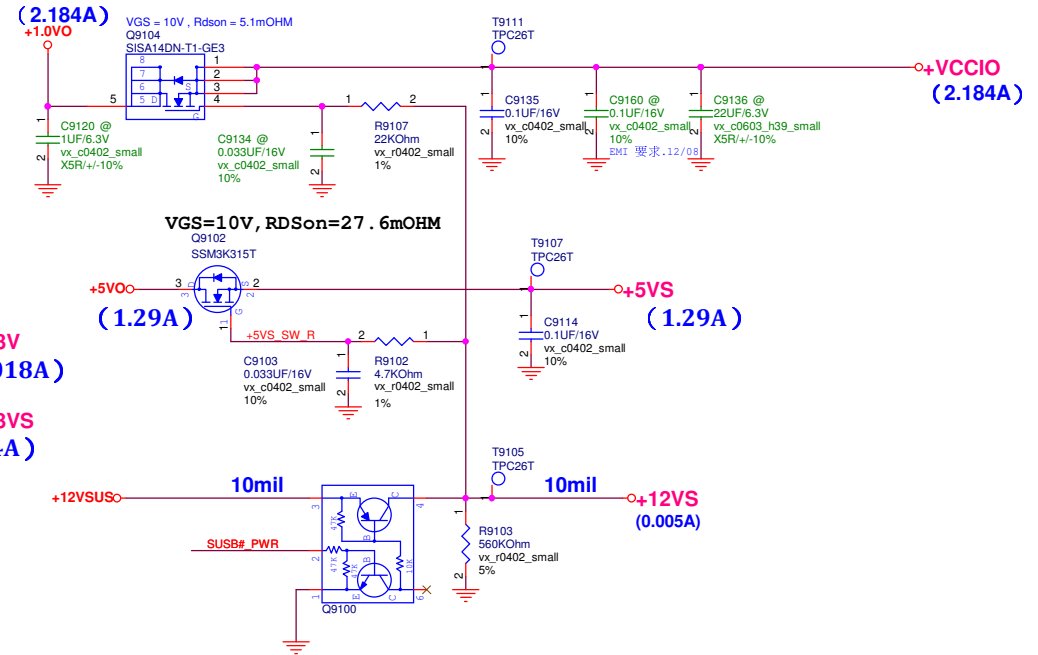


## SUSC#\_PWR POWER Control

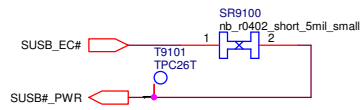


## SUSB#\_PWR POWER

VGS = 10V, Rdson = 5.1mOHM



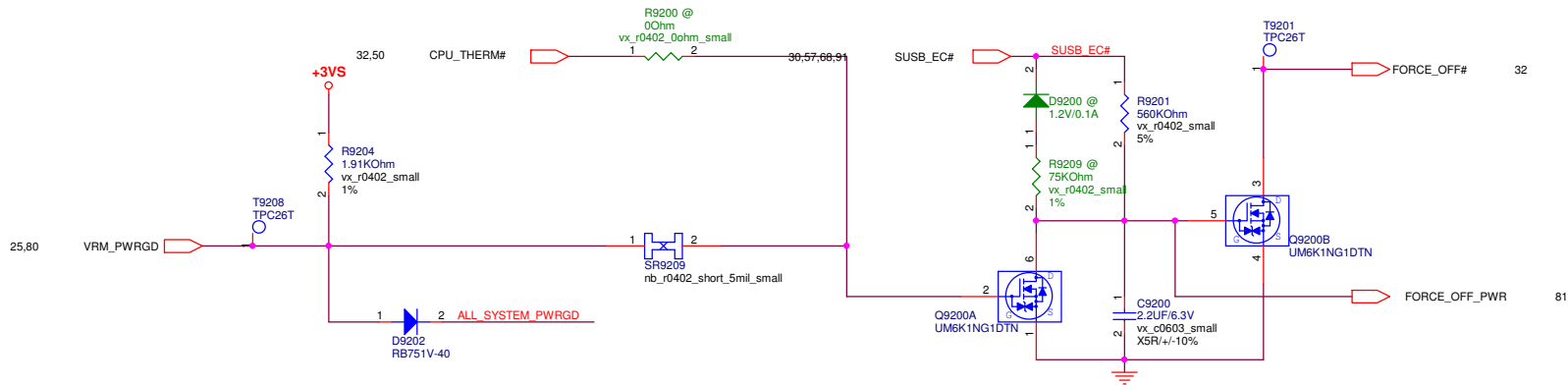
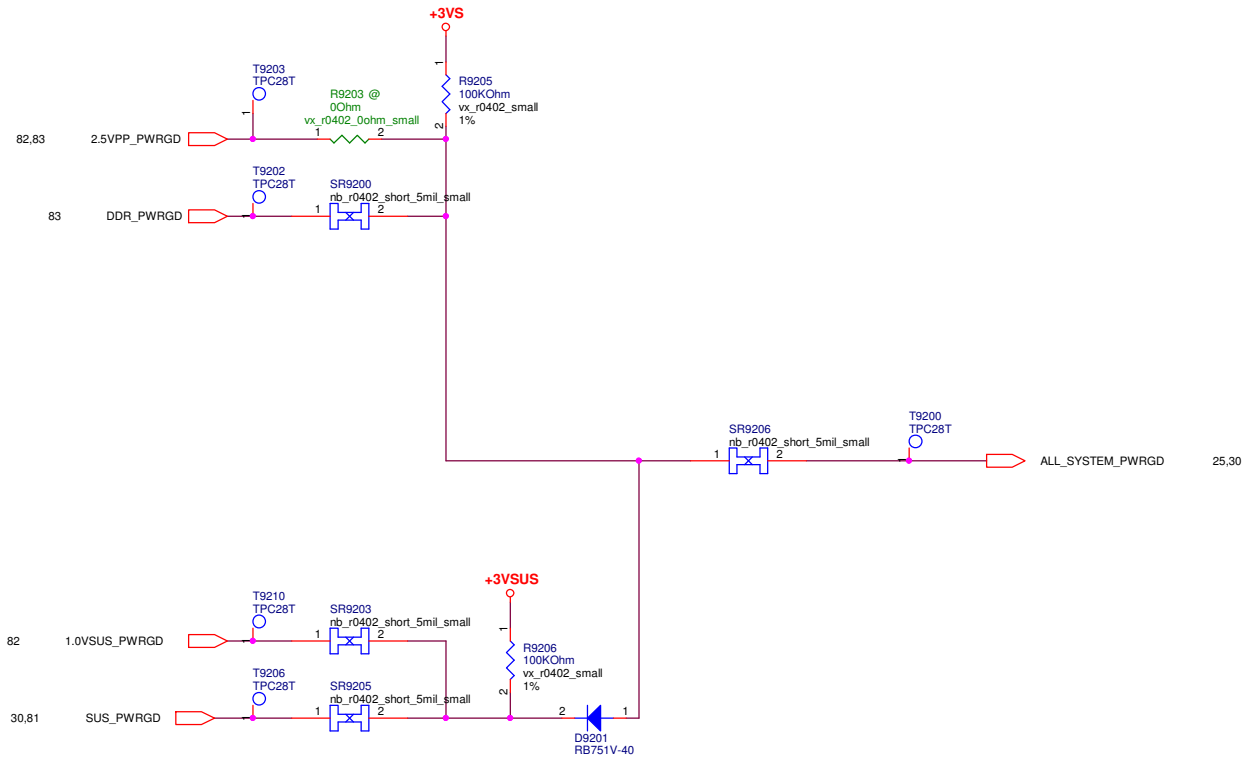
## SUSB#\_PWR POWER Control



<Variant Name>

<b>PEGATRON</b>		Title : <b>POWER_LOAD SWITCH</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer:		Adams Lin	
Size Custom	Project Name  <b>X3</b>	Rev  <b>1.1</b>	
Date:	Wednesday, August 31, 2016	Sheet	91 of 94

# POWER GOOD DETECTOR

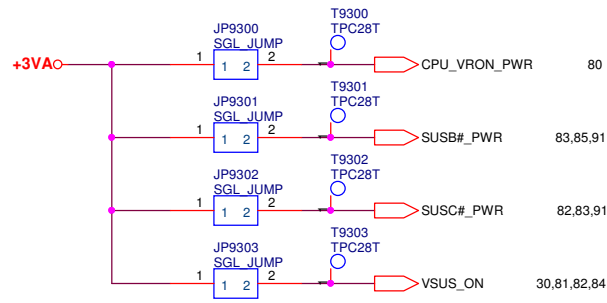


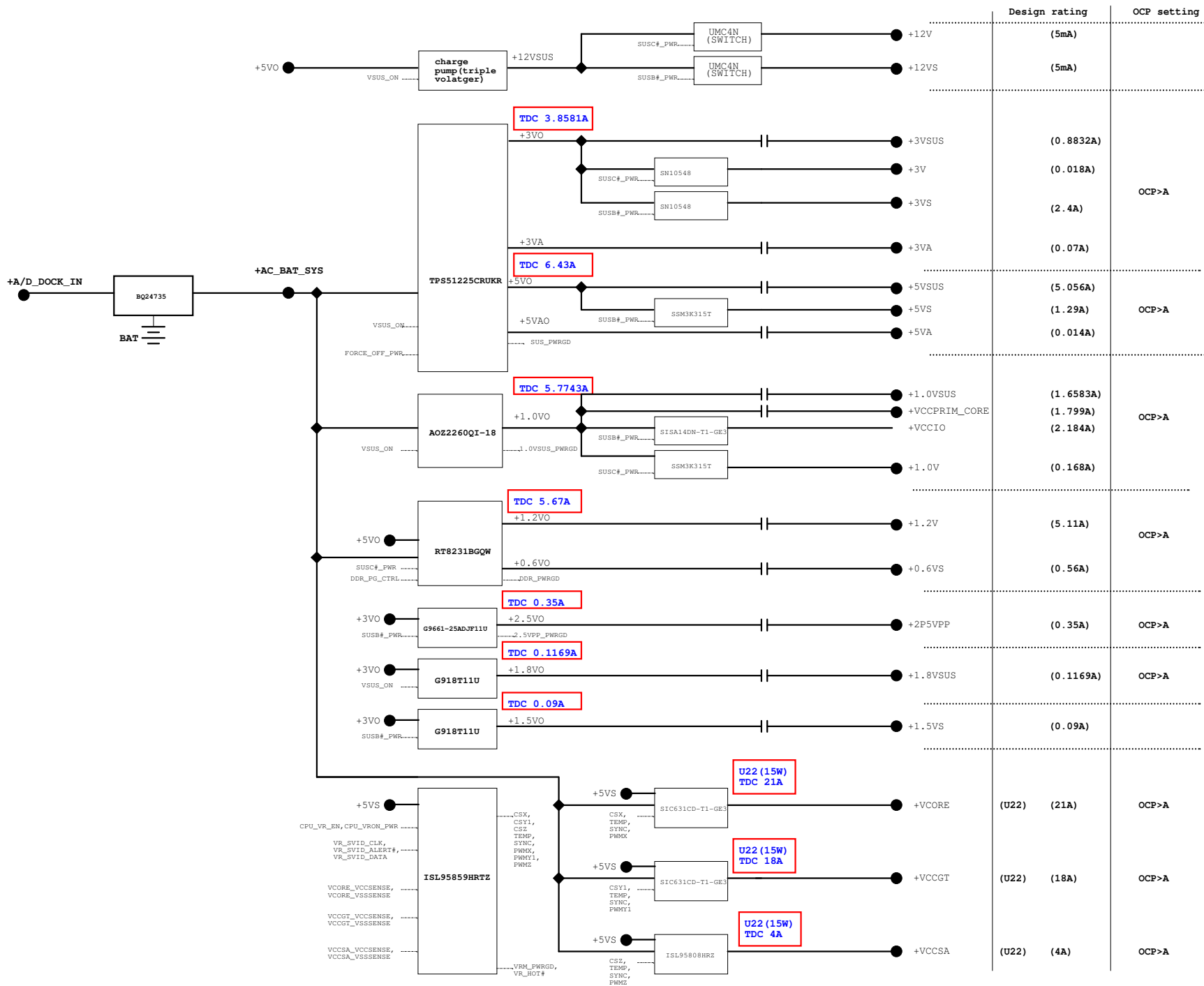
<Variant Name>

<b>PEGATRON</b>		Title : <b>POWER_PROTECT</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: <b>Adams Lin</b>	
Size Custom	Project Name <b>X3</b>	Rev 1.1	
Date: <b>Wednesday, August 31, 2016</b>	Sheet <b>92</b>	of <b>94</b>	

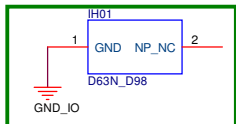
+USB_PD_IN	→	+USB_PD_IN	42,89
+A/D_DOCK_IN	→	+A/D_DOCK_IN	60,89
+AC_USBDPD_WCT_IN	→	+AC_USBDPD_WCT_IN	88,89
+AC_BAT_SYS	→	+AC_BAT_SYS	43,45,80,81,82,83,88
+BAT_CON	→	+BAT_CON	60,88
+RTC_POWER	→	+RTC_POWER	81
+5VA	→	+5VA	31,56,81
+3VA	→	+3VA	24,30,31,36,41,43,53,57,64,81,88
+5VO	→	+5VO	26,81,82,83,88,91
+3VO	→	+3VO	81,82,84,85,91
+2.5VO	→	+2.5VO	82
+1.8VO	→	+1.8VO	84
+1.2VO	→	+1.2VO	83
+1.0VO	→	+1.0VO	82,91
+0.6VO	→	+0.6VO	83
+12VSUS	→	+12VSUS	28,81,91
+5VSUS	→	+5VSUS	41,42,52,56,64,81
+3VSUS	→	+3VSUS	4,24,25,26,28,30,31,41,42,51,53,62,64,68,81,92
+1.8VSUS	→	+1.8VSUS	9,21,22,26,84
+1.0VSUS	→	+1.0VSUS	26,82
+12V	→	+12V	57,91
+2P5VPP	→	+2P5VPP	16,17,57,82
+1.2V	→	+1.2V	4,7,15,16,17,19,57,83
+1.0V	→	+1.0V	7,57,91
+12VS	→	+12VS	31,48,57,91
+5VS	→	+5VS	31,36,45,48,50,51,57,80,91
+3VS	→	+3VS	3,4,21,22,23,24,30,31,32,36,37,44,45,47,50,51,53,57,62,64,91,92
+0.6VS	→	+0.6VS	15,57,83
+VCORE	→	+VCORE	5,80
+VCCGT	→	+VCCGT	6,80
+VCCSA	→	+VCCSA	7,80
+VCCIO	→	+VCCIO	3,7,9,57,91
+VCCPRIM_CORE	→	+VCCPRIM_CORE	26,82

# FOR POWER TEST

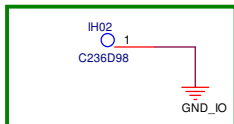




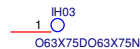
Design rating	OCP setting
(5mA)	
(5mA)	
(0.8832A)	
(0.018A)	
(2.4A)	OCP>A
(0.07A)	
(5.056A)	
(1.29A)	OCP>A
(0.014A)	
(1.6583A)	
(1.799A)	OCP>A
(2.184A)	
(0.168A)	
(5.11A)	OCP>A
(0.56A)	
(0.35A)	OCP>A
(0.1169A)	OCP>A
(0.09A)	
(U22) (21A)	OCP>A
(U22) (18A)	OCP>A
(U22) (4A)	OCP>A



2016.6.6 R1.2\_10L ---For ME

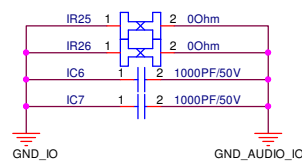
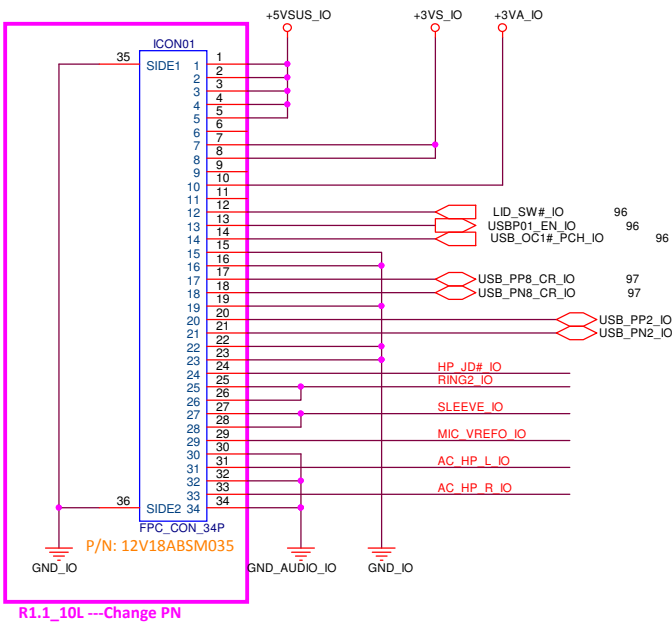
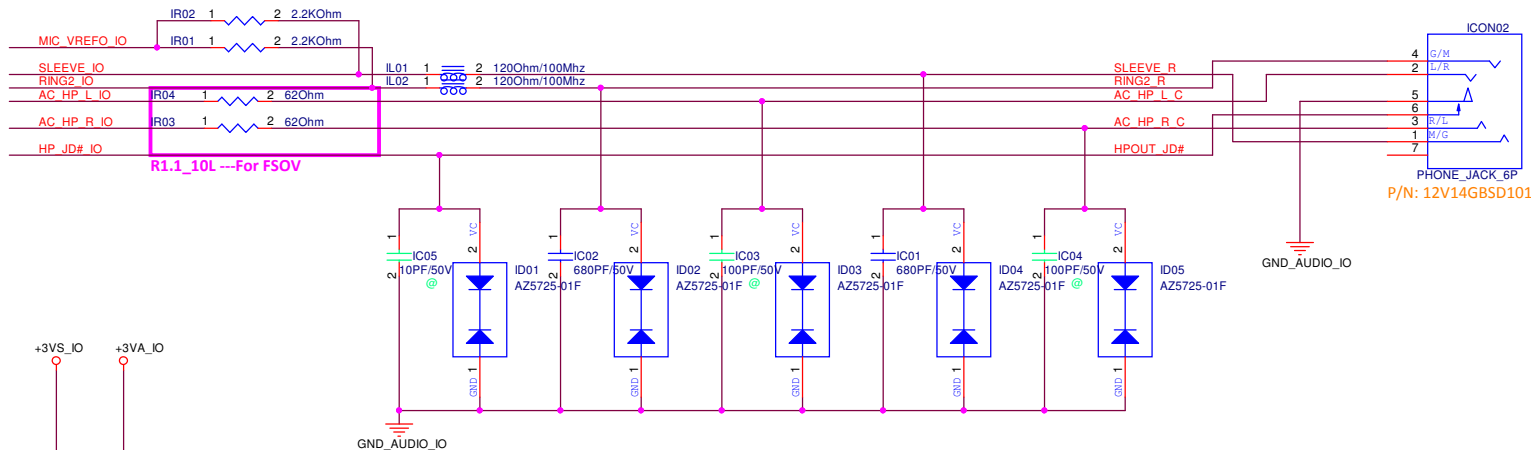


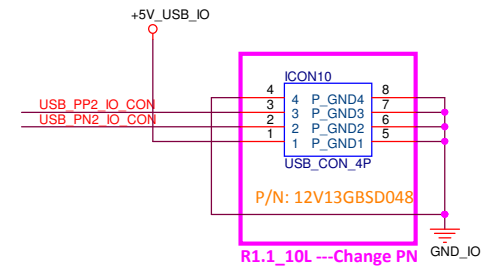
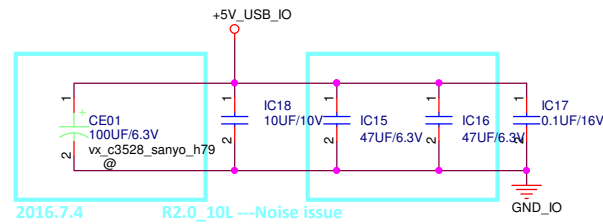
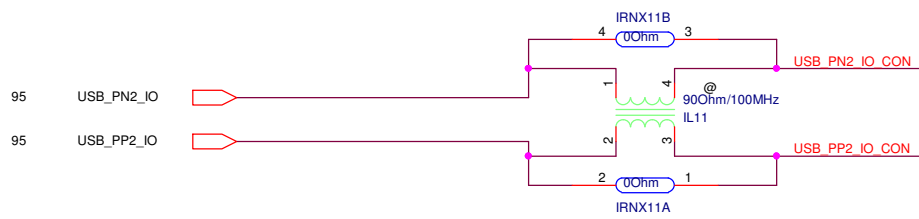
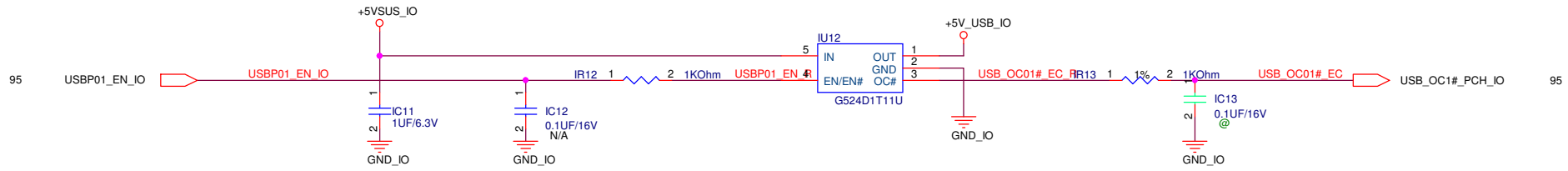
2016.6.6 R1.2\_10L ---For ME



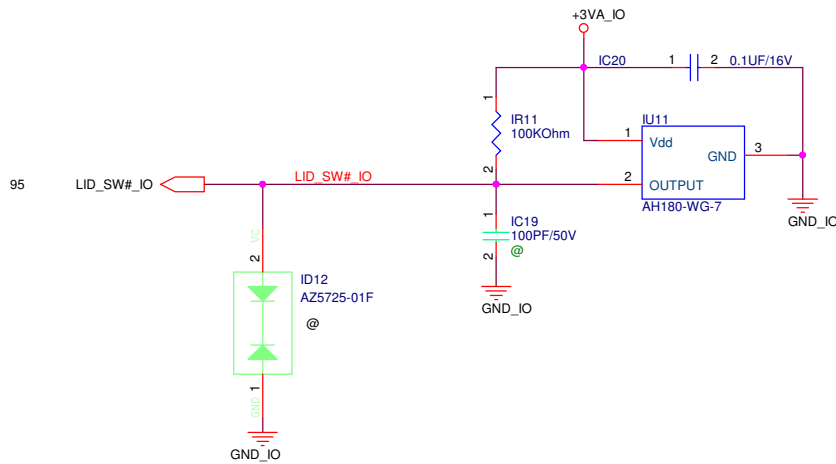
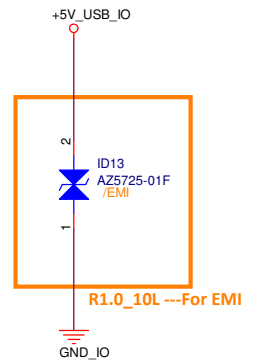
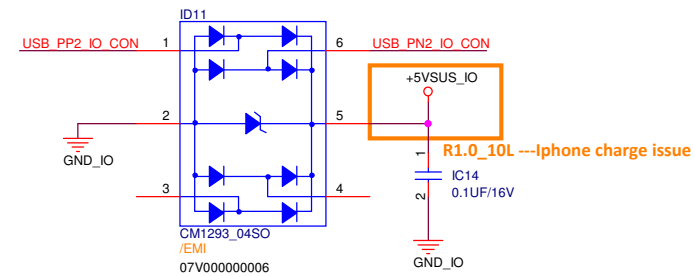
2016.7.14 R1.2\_10L ---For ME

## AUDIO JACK





PLACE ESD Diodes near USB Connector



<b>PEGATRON</b>		<b>Title : USB30_IO_CONN</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		<b>Engineer: Andy Kao</b>	
Size B	Project Name <b>X3</b>	Rev <b>1.0</b>	
Date: <b>Wednesday, August 31, 2016</b>		Sheet <b>96</b> of <b>97</b>	

Cardreader

